EE610A: Analog VLSI Circuits

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PROBLEM SET 4

1) : Fig. 1 shows two current mirrors, without and with cascoded transistors. Both the current sources supply a current of 0.5 mA. Consider $\mu C_{ox} = 100\,\mu$A/V^2, $V_{tn} = 1V$, $\lambda = 0.1$/V, and $W/L = 10$ for all the transistors.

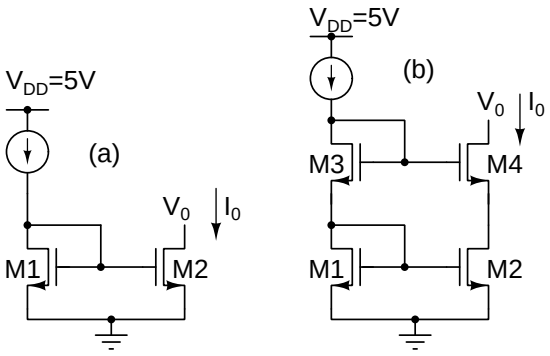

Fig. 1: Problem 1

For the configurations of (a) and (b) find out the following:

(i) What is the minimum value of V_0 for which all the transistors are in saturation?

(ii) In (a) find V_0, for which $I_0 \equiv 0.5\,mA$. What is the minimum and the maximum output current, I_0, when V_0 varies between its minimum possible value and V_{DD}? How does the result vary if you choose to approach it using the exact model vs the incremental model? What is reason behind the difference in values?

(ii) In (b) find V_0, for which $I_0 \equiv 0.5\,mA$.

(iii) What is the minimum and the maximum output current, I_0, when V_0 varies between its minimum possible value and V_{DD}? (Use incremental model.) How does the variation in current compare to (a)? Why?

(iv) Sketch the incremental output resistance at V_0 as a function of the quiescent V_0. Vary V_0 from V_{DD} to 0.

(v) Assume that there is a capacitor attached to the source of M_4. Sketch the incremental output impedance (magnitude), as you increase the frequency from dc to infinite. Assume that all the transistors are in saturation. At what frequency does the impedance starts to change from its dc value, significantly. What is the output impedance at very large frequency. What is the intuition behind the plot?

2) : Fig. 2 shows another rendition of a current mirror. Assume $(W/L)_{M1-4} = 10$. Using the device parameters of problem 1, find out the following:

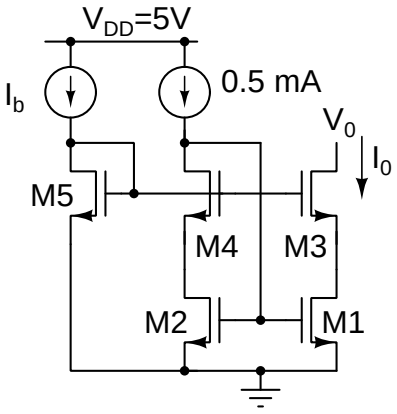

Fig. 2: Problem 2

(i) What is the minimum allowable voltage V_0 for which all the transistors remain in saturation? Assume identical overdrives for $M1-4$.

(ii) What is the variation of the output current I_0 when V_0 varies between its minimum and its maximum of $V_{DD} = 5$ V.

(iii) Find I_b and $(W/L)_{M5}$. Is the solution unique?

(iv) What is the advantage of this mirror over the current mirrors of Fig. 1.

(v) If I_b changes by 10%, how much does I_0 change by? Argue your results using intuition.f

3) : The pMOS transistors, $M3,4$ in Fig. 3 are identical, having aspect ratio of $W3/L3$. $M1$ and $M2$ have aspect ratios of $W1/L1$ and $W2/L1$. Neglect channel length modulation for this problem. Assume non-zero current in both the branches.

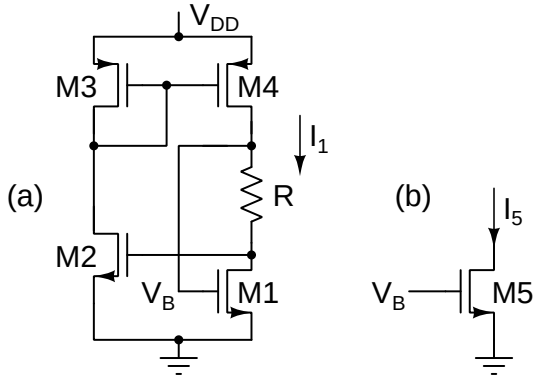

Fig. 3: Problem 3

(i) Find out the current in both the branches in terms of μC_{ox}, V_{tp}, V_{tn}, and W/L of the transistors and R.

(ii) What are the transconductances of $M1$ and $M2$.

(iii) What is the minimum V_{DD} required for this circuit to operate?

(iv) Assume that V_B is used to bias a common source amplifier (b), whose source is grounded. Assume $M5$ is identical to $M1$. What is the transconductance of $M5$? How does the transconductance change with a change in mobility of the device? What is the usefulness of this circuit?

4) : I decided to modify a current mirror circuit by inserting a cascode transistor as shown in Fig. 4.

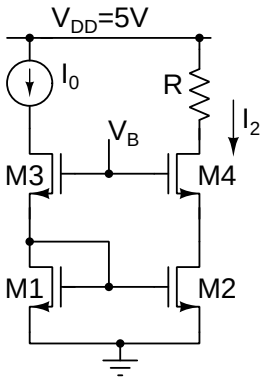

Fig. 4: Problem 4

Ignore channel length modulation. Use the parameters of Question 1. $R = 100\,\Omega$.

(i) How will you set the bias V_B?

(ii) What happens if V_B changes by 100 mV?

(iii) Will this configuration work? Why or why not?