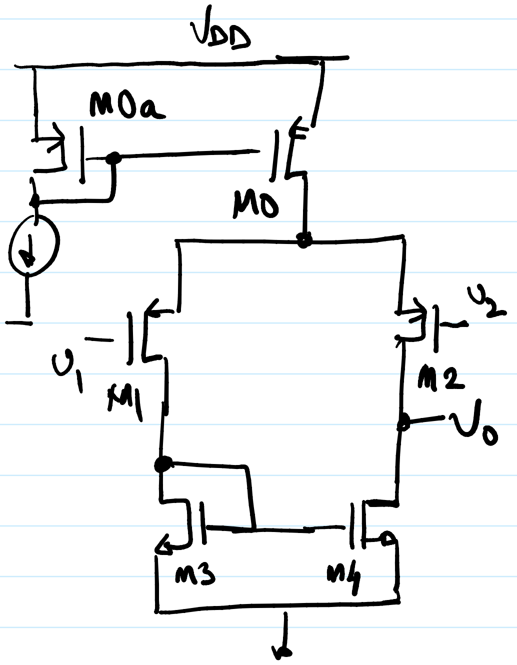
HA5

05 November 2022 09:07

1



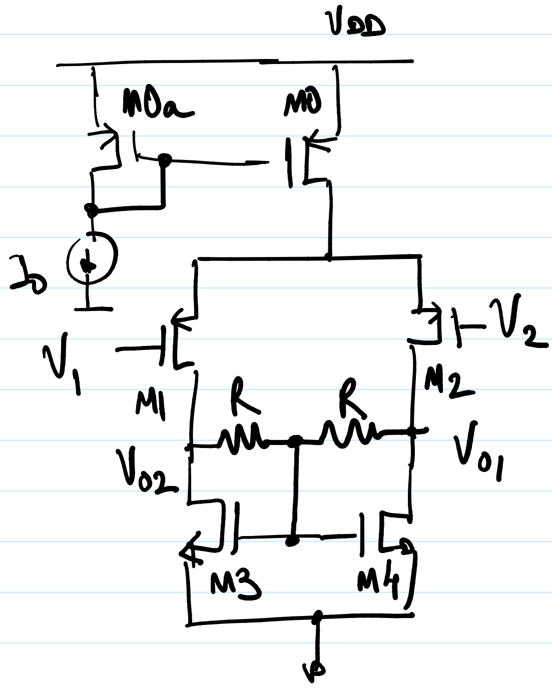
(a) Use the p-input differential pair in a feedback loop to obtain a closed loop gain of −2. You may use one coupling capacitor to isolate the DC-bias and the ac-input if necessary.

(b) Find the steady state error. Make appropriate assumptions on g_{ds} of the transistors.
(Hint: $g_m \gg g_{ds}$ and $g_{ds} \gg 0$)

(c) What is the minimum V_{DD} required to keep all the transistors in saturation.

(d) Find (i) v_o/v_{dd} and (ii) v_o/v_{gnd} for the same configuration (ie under negative feedback).
For (i) neglect the g_{ds} of all transistors other than M0
For (ii) neglect the g_{ds} of all transistors other than M3 and M4.

(2)

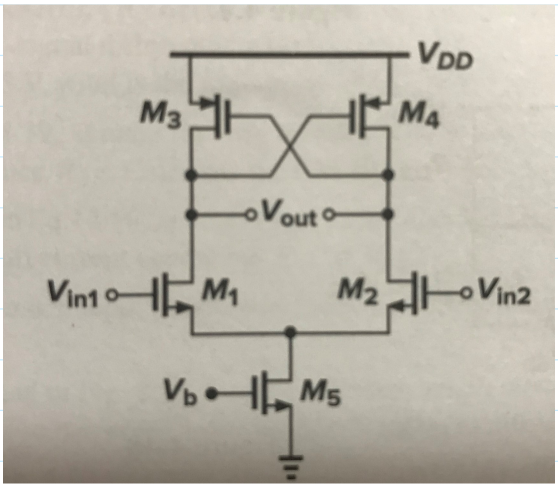


$M1 \equiv M2$ $M3 \equiv M4$

(a) Find expressions for A_d and A_{cm}

(b) Find the $ICMR^+$ and $ICMR^-$ for this configuration.

(3)

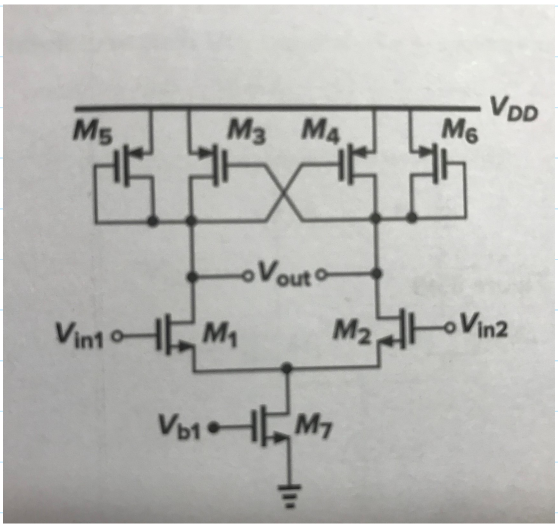


Consider the figure on the left (taken from Analog CMOS Integrated Ckts by B. Razavi)

(a) Considering the g_{ds} of M1 – M5, find A_d and A_{cm}.

(b) Find $ICMR^+$ and $ICMR^-$.

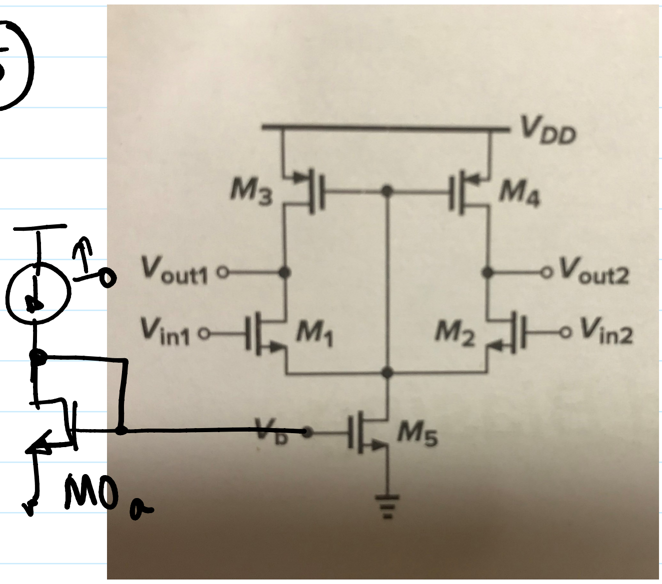
(4)



(a) Find A_d and A_{cm}.
(Neglect g_{ds})

(b) Find $ICMR^+$ and $ICMR^-$

(5)



$V_{DD} = 1.8V$ $\quad I_0 = 200\mu A$

$\mu_n C_{ox} = 200\mu A/V^2$

$\mu_p C_{ox} = 100\ \mu A/V^2$

$V_{thn} = 0.5V, \quad V_{thp} = -0.5V$

$(W/L)_{MOa,\,M5} = 4.$

$(W/L)_{M_1,M_2} = 2$

(a) Find the minimum common mode input voltage for M1, M2, M5 to be in saturation

(b) Size M3 and M4 so that they are at the edge of saturation region.

(c) Find $\dfrac{V_{out_1} - V_{out_2}}{V_{in_1} - V_{in_2}}$ while neglecting g_{ds} of M5.