MOSFET Biasing and Voltage Swings

With current source/mirror

Nagarjuna Nallam

Department of Electrical Engineering
IIT Kanpur, India

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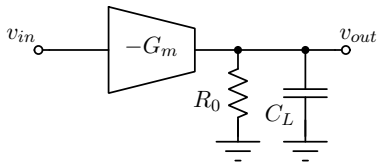
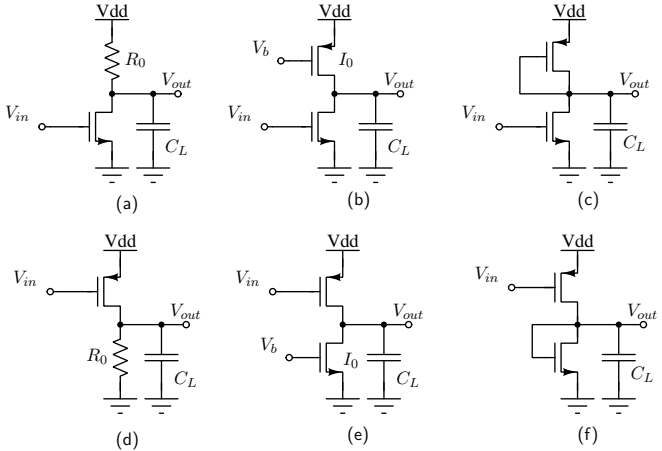
Introduction

Design of a CS amplifier



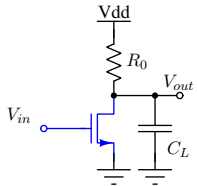
- Design a single stage CS amplifier with a gain-bandwidth (GBW) product of 10^9 Hz while driving a load capacitance of 1 pF.
- Since GBW $= \frac{G_m}{2\pi C_L}$, we can compute G_m required to be 6.28 mS.
- Note that we wanted to design an amplifier that works from DC. So, avoid ac-coupling at the input/output.

The choices for a common source amplifier



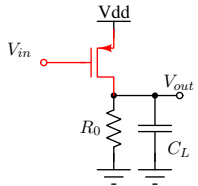
- How to chose between NMOS and PMOS G_m stages and how to chose the load type?

Choosing between NMOS/PMOS G_m stage



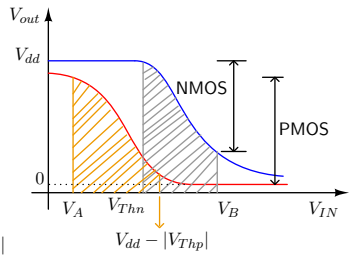
Inversion: $V_{IN} > V_{Thn}$

Saturation: $V_{OUT} > V_{IN} - V_{Thn}$



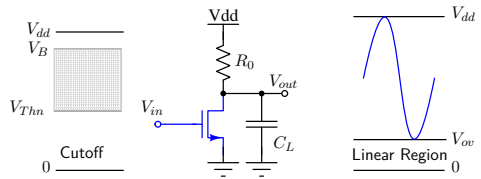
Inversion: $V_{IN} < V_{dd} - |V_{Thp}|$

Saturation: $V_{OUT} < V_{IN} + |V_{Thp}|$



- Both NMOS and PMOS CS stages will have inverting characteristics as shown. The difference is in the input DC voltage level at which the the transistors are in saturation.
- PMOS CS works for small input dc voltage levels, from V_A to $V_{dd} - |V_{Thp}|$, and NMOS CS works for higher dc voltage levels, V_{Thn} to V_B.

Maximum output voltage swing



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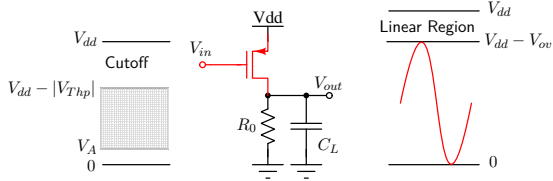
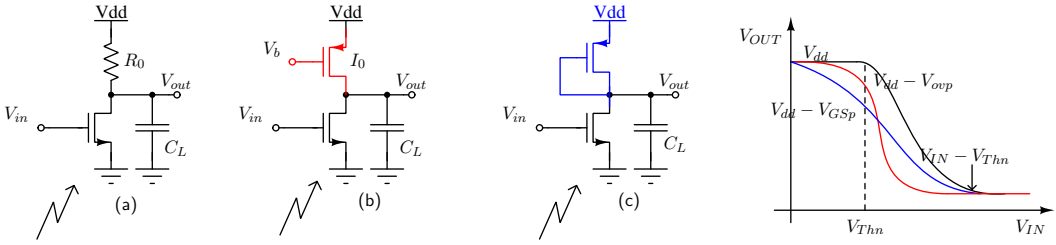


Inversion: $V_{IN} < V_{dd} - |V_{Thp}|$

Saturation: $V_{OUT} < V_{IN} + |V_{Thp}|$

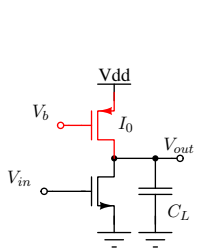
- To find the maximum output swing, check the minimum voltage needed looking down and the maximum voltage we can reach while looking up from the output node while maintaining all transistors in saturation.
- In the NMOS CS stage, the MOSFET needs atleast V_{ov} across it to remain in saturation. On high-side, the resistor doesn't impose any limit. Therefore the maximum swing is from $V_{ov} = V_{IN} - V_{Th}$ to V_{dd}.
- Similarly, the maximum output swing in the PMOS CS is from 0 V to $V_{dd} - V_{ov} = V_{dd} - [V_{dd} - V_{IN} - |V_{Thp}|] = V_{IN} + |V_{Thp}|$.

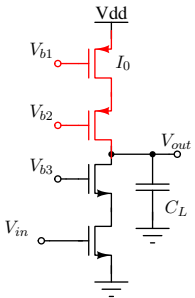
Type of load



- The choice of load type depends largely on what to maximize, primarily, among - voltage gain, bandwidth, and output swing.
- In the above three configurations, the maximum output values possible are V_{dd}, $V_{dd} - V_{ov}$ and $V_{dd} - (V_{Thp} + V_{ov})$, respectively.

High gain stages

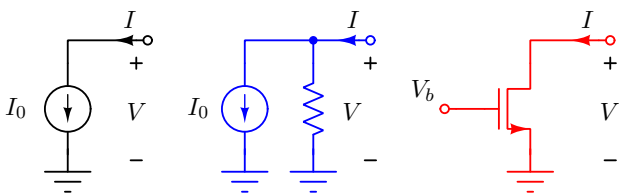


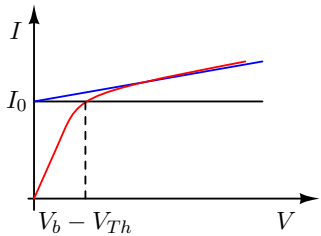


- How to choose the bias voltages $V_{b1,2,3}$ for cascodes and current sources?
- What is the maximum voltage swing we can achieve with these cascode stages?

Current source/mirrors

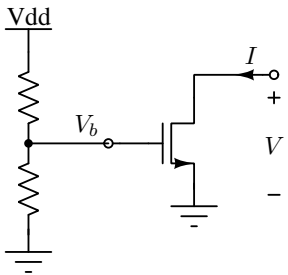
A current sink

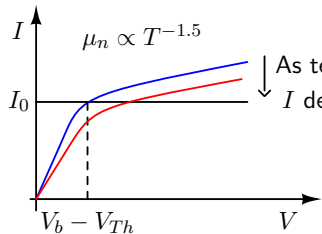


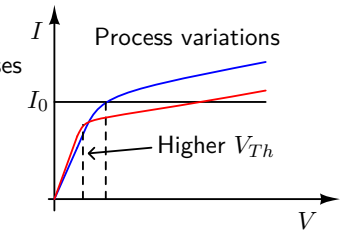


- A MOSFET based current source suffers from two non-idealities: (a) It requires a non-zero minimum voltage across it, and (b) has a finite incremental output impedance

Generation of bias voltage for current source

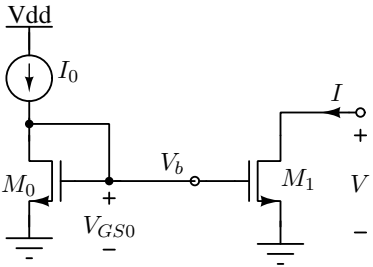






- If we apply a fixed voltage V_b, then the current varies a lot with process and temperature.
- For a good current source, we need to generate V_b such that it tracks the V_{Th} variations and temperature!

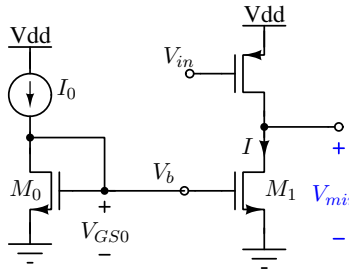
Generation of bias voltage using current mirror



$$V_b = V_{GS0} \approx V_{Th0} + \sqrt{\frac{2I_0}{\mu_n c_{ox}(W/L)_0}}; \quad I \approx 2I_0 \frac{(W/L)_1}{(W/L)_0}$$

- We can use a MOS diode to generate a V_{GS} that tracks the process and temperature variations assuming a golden current reference source is available.
- If M_0 and M_1 are matched transistors, then the current I is a scaled version of I_0. Moreover, the scaling factor, $\frac{(W/L)_1}{(W/L)_0}$, is independent of any technology parameters.

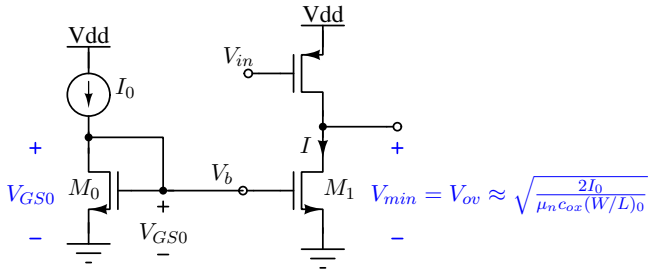
A note V_{min} and output swing



$$V_b = V_{GS0} \approx V_{Th0} + \sqrt{\frac{2I_0}{\mu_n c_{ox}(W/L)_0}}; \quad I \approx I_0 \frac{(W/L)_1}{(W/L)_0}$$

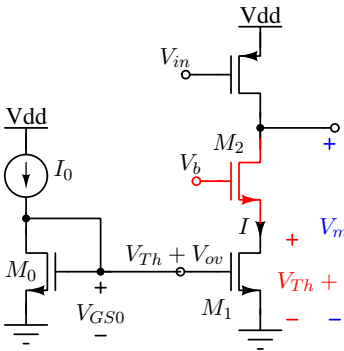
- Note that the absolute value of V_b also matters as it limits the output voltage swing when used in an amplifier.
- We need to choose appropriate dimensions such that V_b is small, typically V_{Th} + 0.1 to 0.2 V.
- The current through M_0 is not contributed to the gain of the amplifier here. Usually I_0 is chosen to be a much smaller than the required I to save power.

Mirroring errors and output resistance



- As the V_{DS} of M_0 and M_1 are not same there will be some mirroring error due to the channel length modulation.
- The channel-length modulation is also the cause of the output resistance.

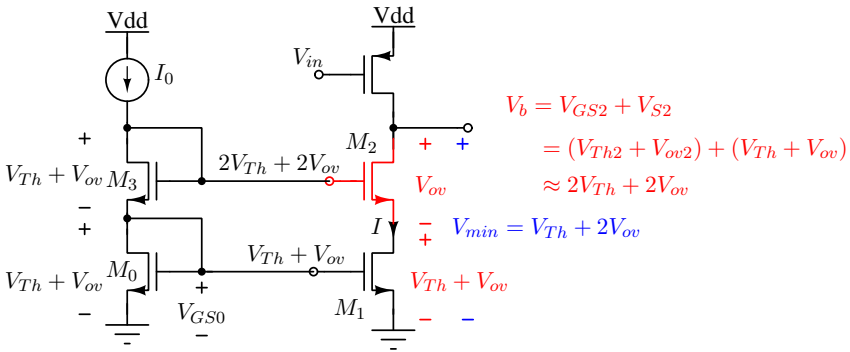
Cascode current source



$$V_b = V_{GS2} + V_{S2}$$
$$= (V_{Th2} + V_{ov2}) + (V_{Th} + V_{ov})$$
$$\approx 2V_{Th} + 2V_{ov}$$

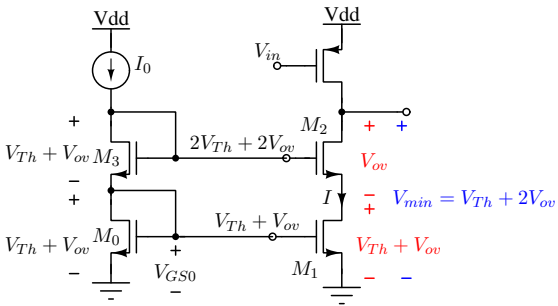
- We can use a cascode source to increase the output incremental resistance.
- Also, if we choose the cascode bias voltage V_b such that $V_{DS1} = V_{DS0} = V_{Th} + V_{ov}$ then the mirroring error can be reduced.
- V_b needed to ensure the above condition is $2V_{Th} + 2V_{ov}$.

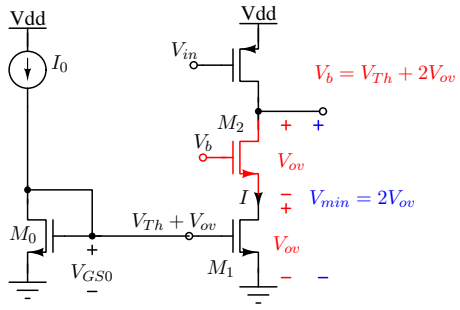
Biasing the cascode current source



- We can easily generate $V_b = 2V_{Th} + 2V_{ov}$ by adding two V_{GS} drops, i.e. by connecting two diodes in series.
- The V_{min} needed for the cascode current source is $V_{G2} - V_{Th} = V_{Th} + 2V_{ov}$.
- Output incremental resistance looking into the cascode drain is $\approx g_{m2} r_{02} r_{01}$.

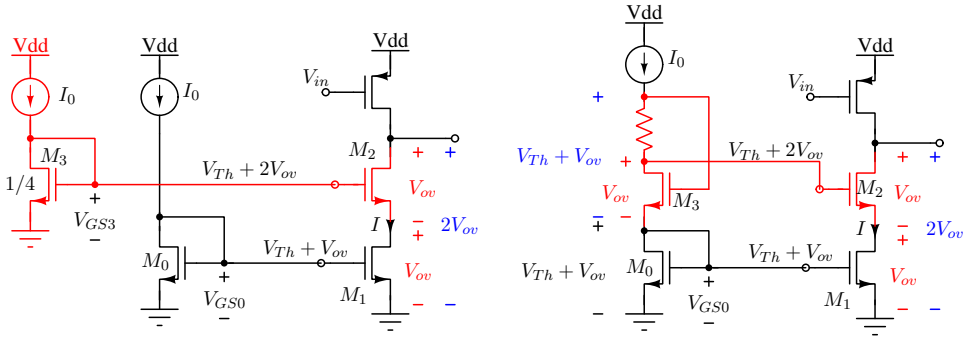
Biasing the cascode current source





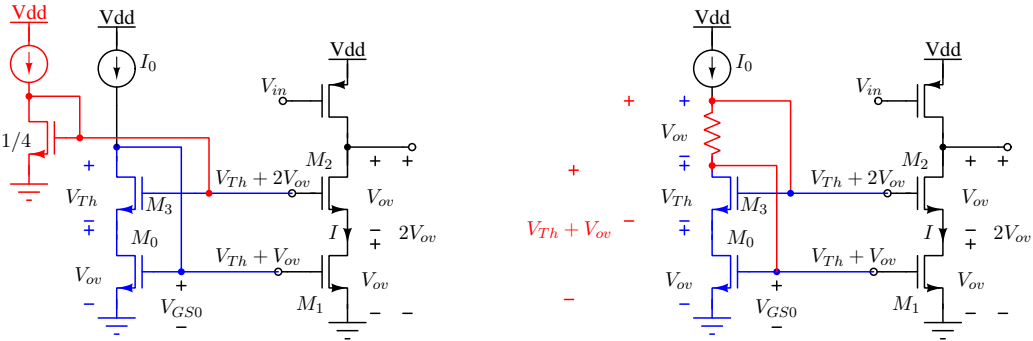
- The cascode discussed previously requires high V_{min} due to V_{Th} and it ultimately limits the output swing in a common source amplifier.
- To achieve large output swing, we need to achieve lowest V_{min} possible, which is $2V_{ov}$. This requires the gate voltage for the cascode to be $V_b = V_{Th} + 2V_{ov}$.

High-swing cascode source



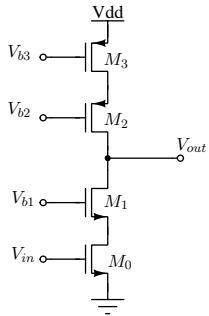
- One way to generate $V_b = V_{Th} + 2V_{ov}$ is by using a diode whose dimensions are $1/4$ compared to M_0. One can also use $4I_0$ instead of smaller diode to generate $2V_{ov}$.
- We can also create one V_{ov} drop by inserting a resistor R into the diode connection as shown in the second circuit. Since the gate is connected at the top of the resistor, $I_0R + V_{DS} = V_{GS3} = V_{Th} + V_{ov}$, and $V_{DS} = V_{ov}$.

High-swing cascode source



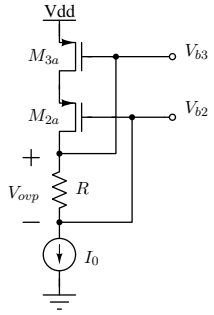
- In the previous architectures, $V_{DS1} \neq V_{DS0}$ which leads to mirroring errors.
- We can resolve this by making the $V_{DS0} = V_{ov}$. The two cascode mirrors seen previously are modified here to ensure $V_{DS0} = V_{DS1} = V_{ov}$.
- If you are confused about M_3 getting V_{Th}, not M_0, check the gate and source voltages. V_{GS} of any transistor in saturation is always $V_{Th} + V_{ov}$, but V_{DS} can be $> V_{DS}$ as per the circuit condition.

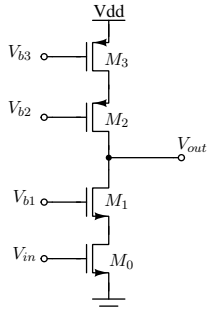
Telescopic Cascode Amplifier

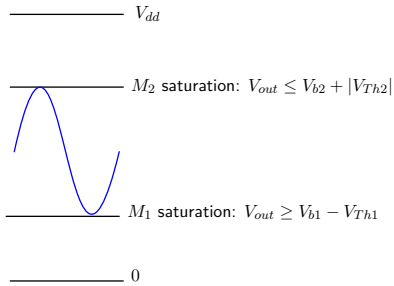


- Find out the bias voltages needed in the telescopic amplifier shown to achieve maximum output swing. What is the maximum output swing possible?
- Design a biasing circuit to generate the gate voltages identified above.

Telescopic Cascode Amplifier

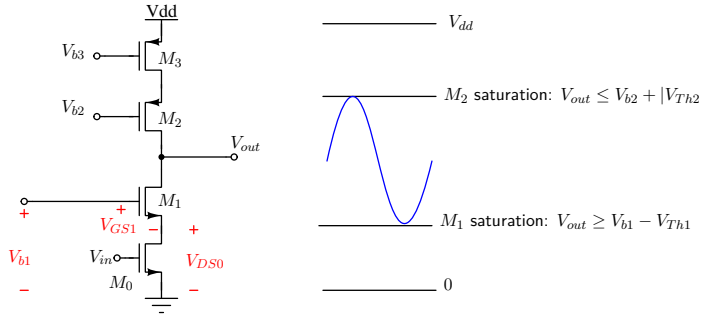






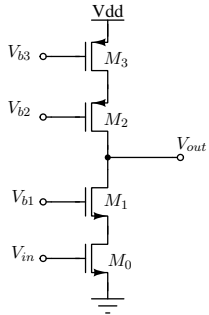
- V_{out} swing is limited by the M_1 and M_2 saturation conditions as shown.
- To achieve maximum output swing, we should design the cascode current source with $V_{min} = 2V_{ov}$. From our previous study, we need $V_{b3} = V_{dd} - (|V_{Thp}| + V_{ovp})$ and $V_{b2} = V_{dd} - (|V_{Thp}| + 2V_{ovp})$ for this. These are the maximum values of V_{b2} and V_{b3}.
- Also, we should chose the device dimensions to minimize V_{ovp} for a given current.

Telescopic Cascode Amplifier



- Again, we can guess that the V_{b1} needed for maximum swing (or smallest V_{min}) is $V_{Th} + 2V_{ov}$. Let us look at other way of deriving this.
- We can write V_{b1} as $V_{GS1} + V_{DS0} = V_{Th1} + V_{ov1} + V_{DS0}$ using voltage drops across transistors. For smallest V_{b1}, we need to operate M_0 at the edge of saturation giving $V_{DS0} = V_{ov0}$. So, minimum V_{b1} is $V_{Th1} + V_{ov1} + V_{ov0}$.
- To maximize the output swing, we should also operate at the smallest V_{IN}.

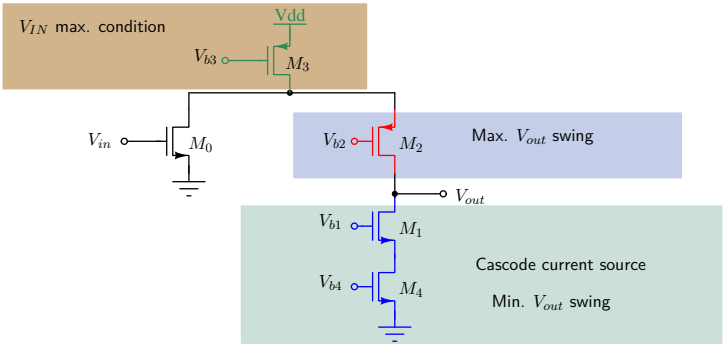
Telescopic Cascode Amplifier



- Let's say, we have chosen V_{b1}, V_{b2} and V_{b3} values (not necessarily for output swing maximization), find out the minim and maximum input DC levels at which the amplifier works.

  Hint: Check the cutoff and saturation conditions for M_0

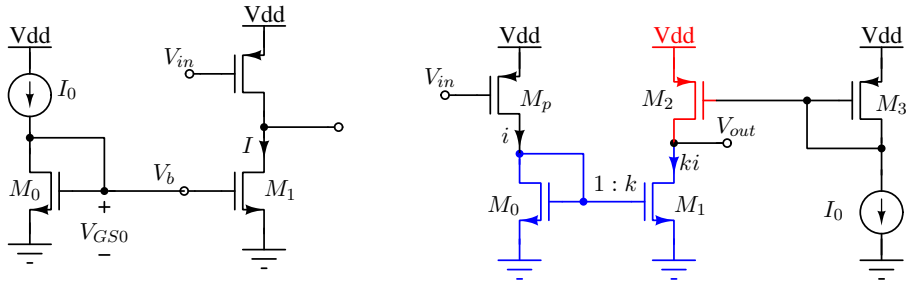
Folded Cascode Amplifier



- Find the maximum output swing limits and input DC levels for proper operation of folded cascode amplifier.
- Draw biasing circuit(s) to generate these voltages from a single current reference.

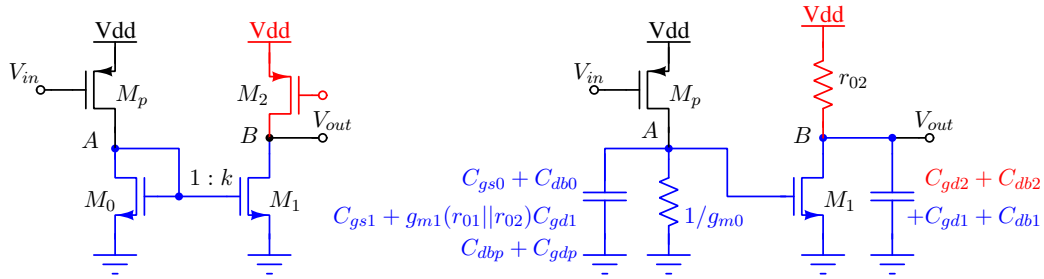
Active mirrors

Can we use mirrors for (current) signal amplification?



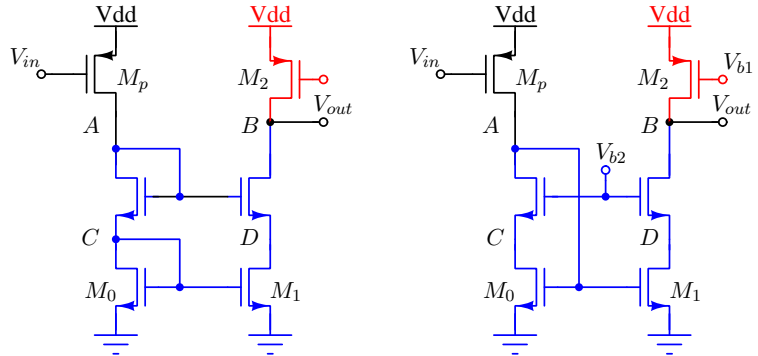
- Yes, we can use the idea of current copying with scaling to signal amplification.
- In (b), M_0 copies the small-signal current generated by M_p to M_1 with a scaling factor of k, i.e., $(W/L)_1 = k(W/L)_0$. The voltage gain of the circuit is $kg_{mp}(r_{01}||r_{02})$.
- Note that the mirror formed by $M_3 - M_2$ is a simple DC current mirror.

Mirror pole



- The mirror node, A, contributes a pole to the system. The resistance at this node, $\approx 1/g_{m0}$, is smaller than the resistance at node B. The capacitance at A could be higher due to C_{gs0}, C_{gs1} and the miller capacitance of M_1.
- Usually, one would design to place the mirror pole at a higher frequency than the output pole.

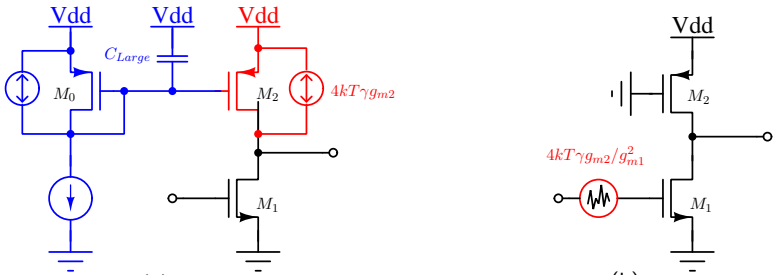
Cascode mirror



- We can also use a cascode mirror for signal processing as shown above. The main reason to use cascode mirror is to increase the output impedance at node B. We can also get additional boost in voltage gain by current scaling in mirror.
- The two additional nodes C and D introduce two more poles, but usually at high frequencies compared to the pole at B.

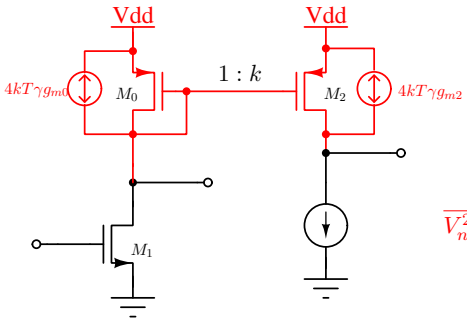
Noise due to current sources/mirrors

Noise due to current source



- The noise due to M_0 can be reduced to a very small value by adding a large capacitance at the gate of M_2 (why?). Adding this capacitance to V_{dd}, rather than to ground, also reduces the supply coupling to the M_2 gate.
- Thermal noise due to M_2 can be referred to the input as $4kT\gamma g_{m2}/g_{m1}^2$. For low noise, one has to reduce g_{m2}. Using small $(W/L)_2$ (or large $(V_{GS2} - V_{Th2})$) can reduce g_{m2}. Note increasing length reduces (W/L) and increases r_0 for a given current.

Noise due to active mirror



$$\overline{V_{n,in}^2} = 4kT\gamma \frac{g_{m0}+g_{m2}/k^2}{g_{m1}^2}$$

- If active mirror is used for signal processing, we can't add extra capacitors without affecting signal performance.
- Here also the g_m of mirror devices should be reduced as much as possible for low noise.

References

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For step-by-step design examples

- Phillip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design," Oxford University Press, 2002.

For a collection of circuit topologies/architectures

- Willy M. C. Sansen, "Analog Design Essentials," Springer-Verlag, Berlin, Heidelberg, 2006.

Thank you!

nallam@iitk.ac.in

https://home.iitk.ac.in/∼nallam/