

EE610: Analog IC Design

Differential Amplifiers: Basics

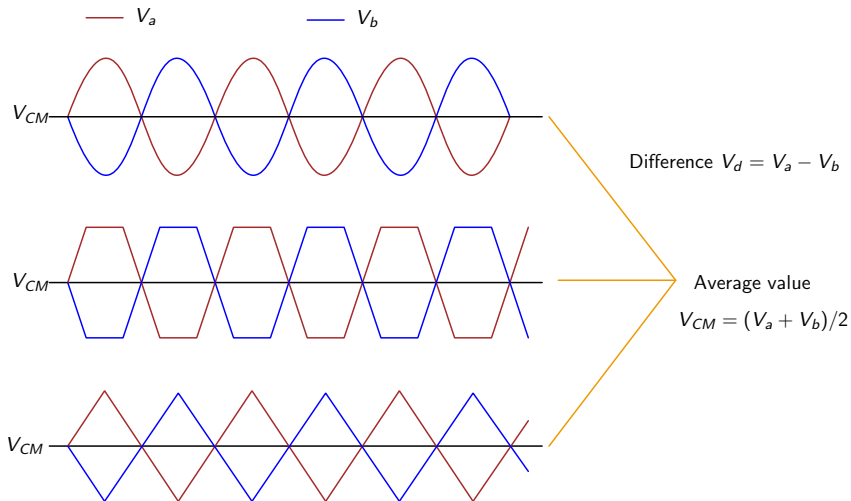
Nagarjuna Nallam

Department of EE, IIT Kanpur, India

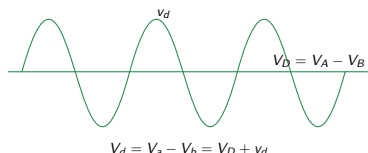
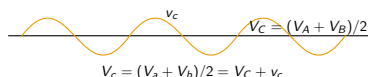
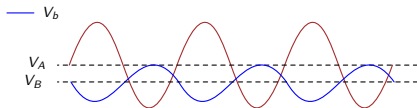
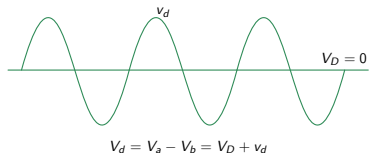
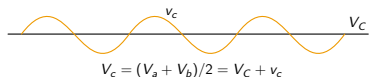
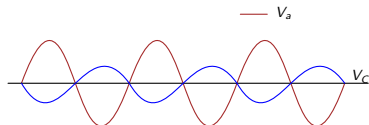
Topics

- ▶ Differential signals and amplifiers
- ▶ Various gains of a differential amplifier
- ▶ A MOS differential amplifier
- ▶ Differential and common-mode equivalent half circuits
- ▶ Large signal characteristics of an nMOS differential pair
- ▶ Effect of device mismatches

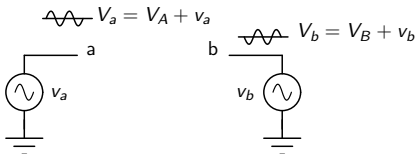
Differential and common-mode signals



Differential and common-mode signals



Differential and common-mode components in two signals

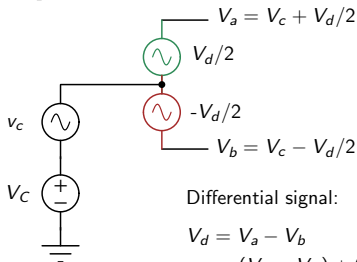


Common-mode signal:

$$V_c = (V_a + V_b)/2$$

$$= (V_A + V_B)/2 + (v_a + v_b)/2$$

$$= V_C + v_c$$

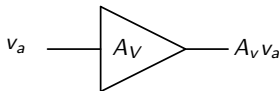


Differential signal:

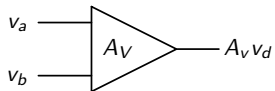
$$V_d = V_a - V_b$$

$$= (V_A - V_B) + (v_a - v_b)$$

Differential amplifier



A single-ended amplifier



A differential amplifier:

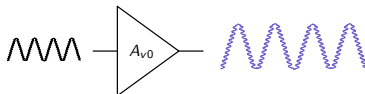
amplifies only the differential signal



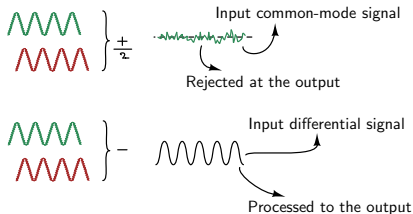
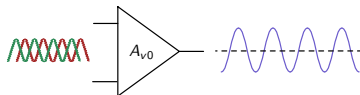
Rejects the common-mode signal/noise/fluctuations present in the input

Advantages of differential signal processing

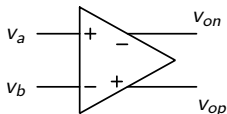
Single-ended signal processing:



Differential signal processing:



A fully-differential amplifier and its gain



A fully-differential amplifier

Let us assume:

$$v_{op} = A_{11}v_a + A_{12}v_b$$

$$v_{on} = A_{21}v_a + A_{22}v_b$$

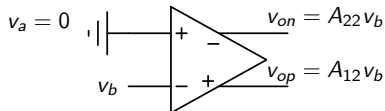
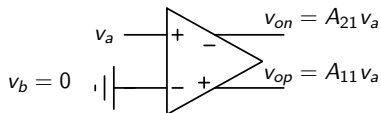
Computation of each coefficient:

$$A_{11} = \left. \frac{v_{op}}{v_a} \right|_{v_b=0}$$

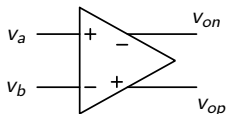
$$A_{12} = \left. \frac{v_{op}}{v_b} \right|_{v_a=0}$$

$$A_{21} = \left. \frac{v_{on}}{v_a} \right|_{v_b=0}$$

$$A_{22} = \left. \frac{v_{on}}{v_b} \right|_{v_a=0}$$



Differential and common-mode gains



A fully-differential amplifier

$$v_a = v_{ic} + v_{id}/2 \quad \left\{ \begin{array}{l} v_{ic} = (v_a + v_b)/2 \\ v_{id} = (v_a - v_b) \end{array} \right.$$

$$v_b = v_{ic} - v_{id}/2$$

$$v_{op} = v_{oc} + v_{od}/2 \quad \left\{ \begin{array}{l} v_{oc} = (v_{op} + v_{on})/2 \\ v_{od} = (v_{op} - v_{on}) \end{array} \right.$$

$$v_{on} = v_{oc} - v_{od}/2$$

A_{dm} : Differential-mode gain

A_{cm} : Common-mode gain

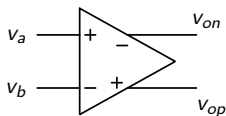
A_{dm-cm} : Differential-mode to common-mode gain

A_{cm-dm} : Common-mode to differential-mode gain

$$v_{od} = A_{dm}v_{id} + A_{cm-dm}v_{ic}$$

$$v_{oc} = A_{dm-cm}v_{id} + A_{cm}v_{ic}$$

Differential and common-mode gains



A fully-differential amplifier

$$v_a = v_{ic} + v_{id}/2 \quad \left\{ \begin{array}{l} v_{ic} = (v_a + v_b)/2 \\ v_{id} = (v_a - v_b) \end{array} \right.$$

$$v_{op} = v_{oc} + v_{od}/2 \quad \left\{ \begin{array}{l} v_{oc} = (v_{op} + v_{on})/2 \\ v_{od} = (v_{op} - v_{on}) \end{array} \right.$$

$$A_{dm} = \frac{A_{11} - A_{12} - A_{21} + A_{22}}{2}$$

$$A_{cm} = \frac{A_{11} + A_{12} + A_{21} + A_{22}}{2}$$

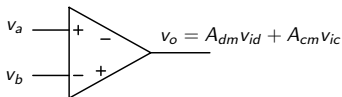
$$A_{dm-cm} = \frac{A_{11} - A_{12} + A_{21} - A_{22}}{4}$$

$$A_{cm-dm} = A_{11} + A_{12} - A_{21} - A_{22}$$

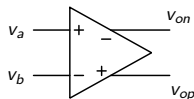
In a balanced differential amplifier, $A_{dm-cm} = A_{cm-dm} = 0$.

Even in a perfectly balanced practical amplifier ($v_{ic} = 0$), $A_{cm} \neq 0$ is possible.

Common-mode rejection ratio (CMRR)



Differential amplifier with single-ended output



Fully-differential amplifier

$$\text{Common-Mode Rejection Ratio (CMRR)} = \left| \frac{A_{dm}}{A_{cm}} \right|$$

Notes:

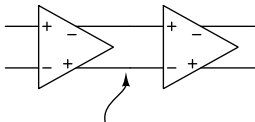
Some references use $\text{CMRR} = \left| \frac{A_{dm}}{A_{cm-dm}} \right|$ for fully-differential circuits.

A_{cm-dm} and A_{dm-cm} are mainly caused by component mismatch.

$A_{cm-dm} = A_{dm-cm} = 0$ for a perfectly balanced circuit.

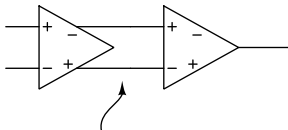
We will stick to $\text{CMRR} = \left| \frac{A_{dm}}{A_{cm}} \right|$ for both the circuits shown above.

CMRR of two stage amplifiers



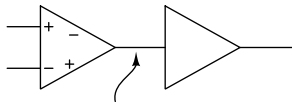
A_{cm-dm} of the first stage limits the overall CMRR

(a)



A_{cm-dm} of the first stage limits the overall CMRR

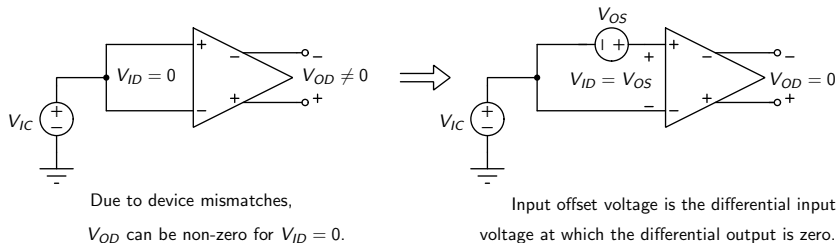
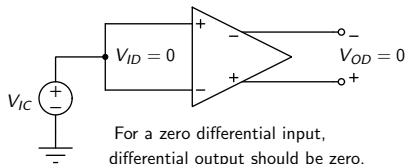
(b)



A_{cm} of the first stage limits the overall CMRR

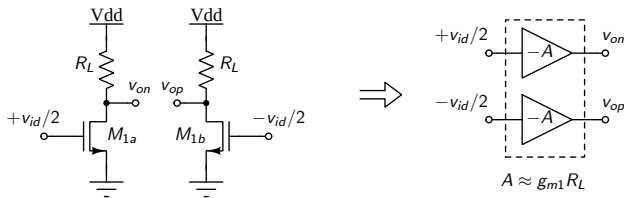
(c)

Input offset voltage



Two single-ended amplifiers to process a differential signal?

Pseudo Differential Amplifier

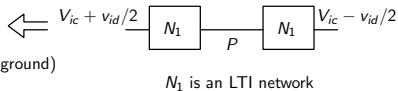
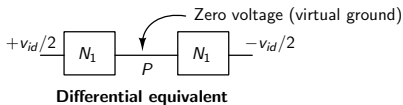
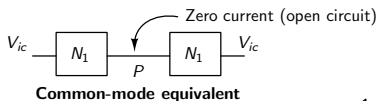
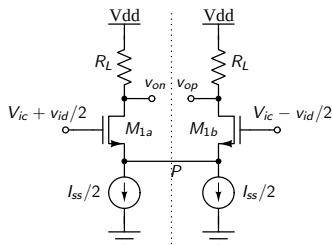
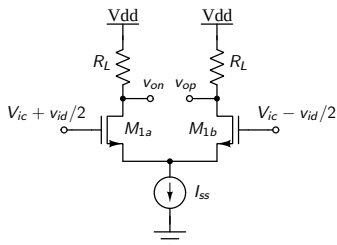


$$A_{dm} = A_{cm} \approx g_{m1} R_L \Rightarrow CMRR = 1$$

Pseudo differential pair can be used for differential signal processing but has poor CMRR!

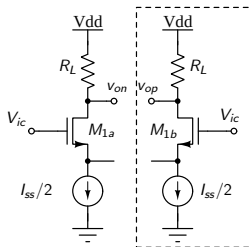
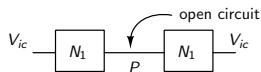
Recall: A differential amplifier is supposed to amplify the differential input only.

An nMOS differential pair: Introduction



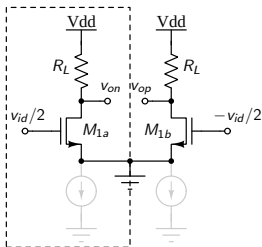
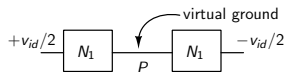
An nMOS differential pair: Equivalent Half Circuits

Common-mode equivalent



CM equivalent half circuit

Differential equivalent

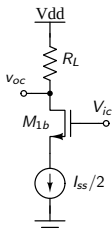


DM equivalent half circuit

The response of the full circuit can be predicted from the equivalent half-circuit(s).

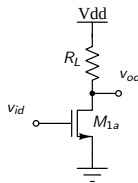
An nMOS differential pair: CMRR

CM equivalent half circuit



$|A_{cm}| \rightarrow 0$ if the current source is ideal.

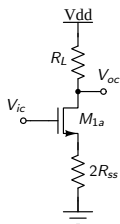
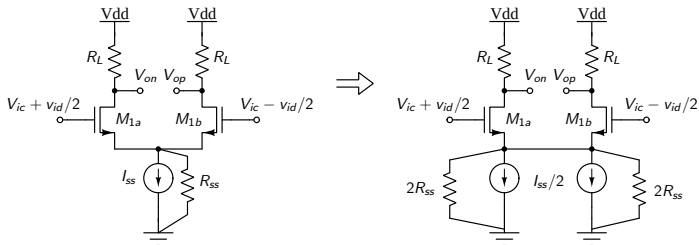
DM equivalent half circuit



$|A_{dm}| \approx g_{m1} R_L$

$\text{CMRR} \rightarrow \infty$

An nMOS differential pair: Effect of tail resistance

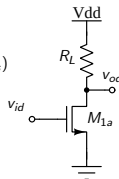


CM equivalent half circuit

$$|A_{cm}| \approx g_{m1} R_L / (1 + 2g_{m1} R_{ss})$$

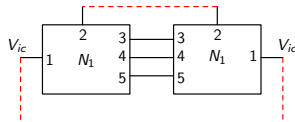
$$|A_{dm}| \approx g_{m1} R_L$$

$$\text{CMRR} \approx 1 + 2g_{m1} R_{ss}$$

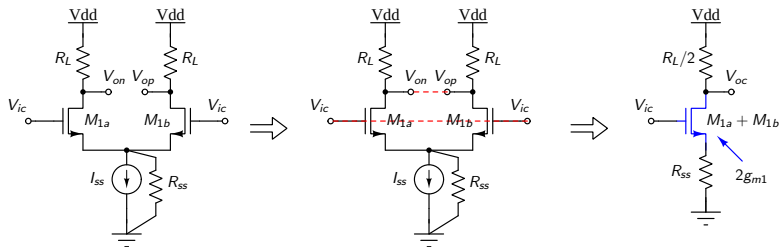


DM equivalent half circuit

Another method to find out the CM response

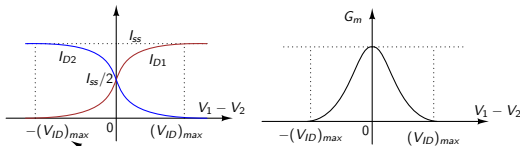
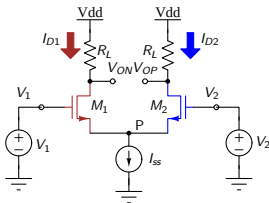


If two identical networks are connected as shown above and excited by a CM signal, then the i^{th} nodes in both the networks will have the same potential. We can short the two i^{th} nodes.



$$|A_{cm}| \approx g_{m1} R_L / (1 + 2g_{m1} R_{ss})$$

An nMOS differential pair: Large-signal DM characteristics



Maximum differential voltage at which $I_{D2} = I_{SS}$

$$V_1 = V_P + V_{TH} + \sqrt{\frac{2I_{D1}}{\mu_n C_{ox} W/L}}$$

$$V_2 = V_P + V_{TH} + \sqrt{\frac{2I_{D2}}{\mu_n C_{ox} W/L}}$$

$$V_1 - V_2 = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox} W/L}} + \sqrt{\frac{2I_{D2}}{\mu_n C_{ox} W/L}}$$

$$I_{D1} = \frac{I_{SS}}{2} + \frac{\mu_n C_{ox} (W/L)(V_1 - V_2)}{4} \sqrt{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - (V_1 - V_2)^2}$$

$$I_{D2} = \frac{I_{SS}}{2} - \frac{\mu_n C_{ox} (W/L)(V_1 - V_2)}{4} \sqrt{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - (V_1 - V_2)^2}$$

$$(V_{ID})_{max} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} W/L}}$$

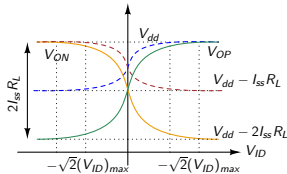
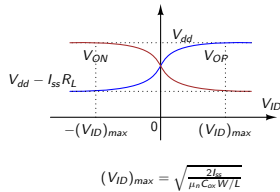
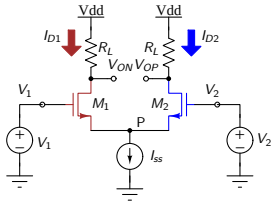
$$= \sqrt{2}(V_{ov})|_{V_{ID}=0}$$

$$V_{ON} = V_{dd} - I_{D1}R_L$$

$$V_{OP} = V_{dd} - I_{D2}R_L$$

$$G_m = \frac{\partial(I_{D2} - I_{D1})}{\partial(V_1 - V_2)}$$

An nMOS differential pair: Large-signal DM characteristics

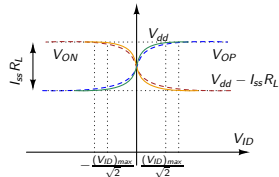


Doubling I_{ss} to increase G_m :

G_m increases by $\sqrt{2}$

Doubles the output swing

Increases the maximum V_{ID} by $\sqrt{2}$



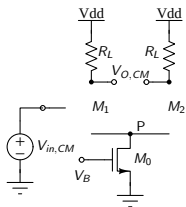
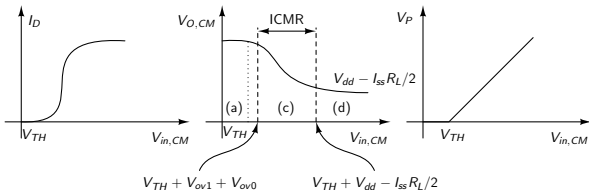
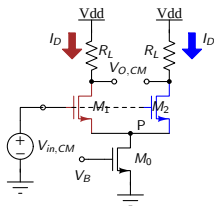
Doubling (W/L) to increase G_m :

G_m increases by $\sqrt{2}$

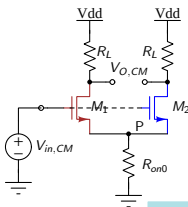
No change in the output swing

Increases the maximum V_{ID} by $\sqrt{2}$

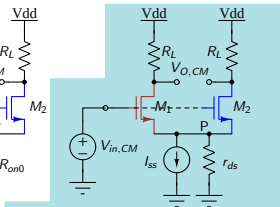
An nMOS differential pair: Large-signal CM characteristics



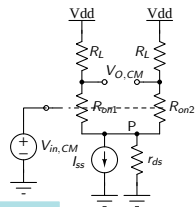
(a) $V_{in,CM} < V_{TH}$



(b) $V_{TH} < V_{in,CM} < V_{GS1} + (V_B - V_{TH})$

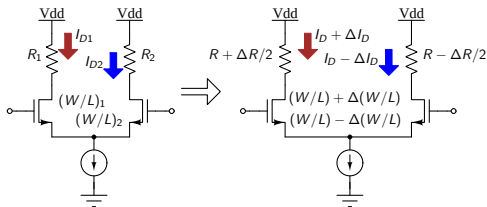


(c) $V_{GS1} + V_B - V_{TH} < V_{in,CM} < V_{DD} - I_{ss}R_L/2 + V_{TH}$



(d) $V_{in,CM} > V_{DD} - I_{ss}R_L/2$

Device mismatches in differential pair: V_{OS}



$$R = (R_1 + R_2)/2$$

$$\Delta R = R_1 - R_2$$

$$(W/L) = ((W/L)_1 + (W/L)_2)/2$$

$$\Delta(W/L) = (W/L)_1 - (W/L)_2$$

$$I_D = (I_{D1} + I_{D2})/2$$

$$\Delta I_D = I_{D1} - I_{D2}$$

$$V_{TH} = (V_{TH1} + V_{TH2})/2$$

$$\Delta V_{TH} = V_{TH1} - V_{TH2}$$

$$V_{GS} - V_{TH} = \sqrt{\frac{2I_D}{\mu_n C_{ox}(W/L)}}$$

Input Offset Voltage: V_{ID} at which $V_{OD} = 0 \Rightarrow I_{D1}R_1 = I_{D2}R_2$

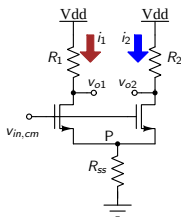
$$V_{OS} = V_{TH1} - V_{TH2} + \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}(W/L)_1}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}(W/L)_2}}$$

$$\approx \Delta V_{TH} + \frac{V_{GS} - V_{TH}}{2} \left(\frac{\Delta I_D}{I_D} - \frac{\Delta(W/L)}{(W/L)} \right)$$

$$\approx \Delta V_{TH} + \frac{V_{GS} - V_{TH}}{2} \left(-\frac{\Delta R}{R} - \frac{\Delta(W/L)}{(W/L)} \right)$$

$$\rightarrow \text{since } I_{D1}R_1 = I_{D2}R_2 \Rightarrow \frac{\Delta I_D}{I_D} = -\frac{\Delta R}{R}$$

Device mismatches in differential pair: A_{cm-dm}



$$i_1 = g_{m1}(v_{in,cm} - v_p) \Rightarrow v_{o1} = -g_{m1}R_1(v_{in,cm} - v_p)$$

$$i_2 = g_{m2}(v_{in,cm} - v_p) \Rightarrow v_{o2} = -g_{m2}R_2(v_{in,cm} - v_p)$$

$$v_p = -\frac{(g_{m1} + g_{m2})R_{ss}}{1 + (g_{m1} + g_{m2})R_{ss}}v_{in,cm}$$

$$v_{o1} = -\frac{g_{m1}R_1}{1 + (g_{m1} + g_{m2})R_{ss}}v_{in,cm}$$

$$v_{o2} = -\frac{g_{m2}R_2}{1 + (g_{m1} + g_{m2})R_{ss}}v_{in,cm}$$

$$v_{od} = -\frac{g_{m1}R_1 - g_{m2}R_2}{1 + (g_{m1} + g_{m2})R_{ss}}v_{in,cm}$$

$$|A_{cm-dm}| = \left| \frac{g_{m1}R_1 - g_{m2}R_2}{1 + (g_{m1} + g_{m2})R_{ss}} \right|$$

Exercise: Find out A_{cm} , A_{dm} , and CMRR.

Summary

- ▶ Differential and common-mode signals
- ▶ Differential amplifiers
- ▶ Different gains: A_{dm} , A_{cm} , A_{cm-dm} , A_{dm-cm} , and V_{OS}
- ▶ DM and CM equivalent half circuits of a balanced fully-differential amplifier
- ▶ Studied the large and small signal characteristics of an nMOS differential amplifier
- ▶ Effect of device mismatches on the circuit performance