SHUBHAM SAHAY

Assistant Professor, IIT Kanpur D.O.B: 23/12/1993
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EMPLOYMENT

Designation	Year	Institution
Assistant Professor	2020-present	**Indian Institute of Technology Kanpur, India**
Post-doctoral Research Scholar	2018-2020	University of California, Santa Barbara, CA, USA

EDUCATION

Degree	Year	Institution	DGPA/Percentage
Ph.D. in Electrical Engineering	2014-2018	Indian Institute of Technology Delhi, India	10.0/10 (rel.)
B.Tech in Electronics Engineering	2010- 2014	Indian Institute of Technology Varanasi	9.11/10 (abs.)
Class XII,AISSCE (CBSE)	2010	D.A.V. Public School, Patna, India	87.0%
Class X, AISSE (CBSE)	2008	D.A.V. Public School, Patna, India	92.6%

rel.: relative grading system abs.: absolute grading system

PROFESSIONAL ACTIVITIES

Member: IEEE

Reviewer: IEEE Transactions on Circuits and Systems I: Regular Papers (**TCAS-I**), IEEE Electron Device Letters (**EDL**),IEEE Transactions on Electron Devices (**TED**), IEEE Transactions on Very Large Scale Integration Systems (**TVLSI**), IEEE Journal of the Electron Devices Society (**JEDS**), IEEE Transactions on Device and Materials Reliability (**TDMR**), IEEE **Access**, IEEE Journal of Exploratory Solid-State Computational Devices and Circuits (**JxCDC**), IEEE **Sensors** Journal,

Elsevier Superlattices and Microstructures, Elsevier Microelectronics Journal**,** Elsevier Cryogenics, IETE Technical Review (**TITR**), Springer Journal of Computational Electronics (**JCEL**), Springer **Applied Physics A**: Materials Science and Processing, IET Circuits, Devices & Systems, IET Micro and Nano Letters.

Conferences: IEEE **EDTM**, IEEE **MWSCAS.**

ACADEMIC DISTINCTIONS

- Appeared in the **list of golden reviewers** for IEEE Transactions on Electron Devices (**TED**) in 2017, 2018 and 2019.
- Awarded I.I.T. (B.H.U.), Varanasi **Gold Medal** for standing **First** at the B.Tech. in Electronics Engineering Examination, 2014.
- Awarded Late Prof. Nagesh Chandra Vaidya **Gold Medal** for standing **First** at the B.Tech. in Electronics Engineering Examination, 2014.
- Awarded Dr. (Late) Nandita Saha Roy Memorial **Gold Medal** for securing **First** position in B.Tech. Electronics Engineering Examination, 2014.
- Awarded C. Raja Gopal Memorial **Gold Medal** for securing **highest marks** (institute highest SGPA of **9.92** in absolute scale) in B.Tech. 4-Year Electronics Engineering Examination, 2014.
- Awarded Dr. Ayyagari Sambasiva Rao Prize Rs. 1000/- cash for standing **First** at the B.Tech. in Electronics Engineering Examination, 2014.
- Awarded Late Prof. Manoranjan Sengupta Platinum Jubilee Merit Award Rs. 1000/- cash for securing **highest marks** in B.Tech. in Electronics Engineering Examination, 2014.
- Got department changed from chemical engineering to electronics engineering on the basis of performance in B.Tech 1st year.
- Secured All India Rank **3894** (out of 400,000 candidates) in IIT Joint Entrance Exam (IIT JEE)-2010.
- **1st** rank in GENIUS- 40 examination held for preparation for IIT JEE and was awarded a laptop in 2010.
- Medha Puraskar from D.A.V committee in X and XII for excellence in board examination and IIT JEE, respectively.
- Selected in Regional Mathematics Olympiad (RMO)in class X and XI for Indian Mathematics Olympiad (IMO).
- Merit certificate under national merit certificate scheme of C.B.S.E (class X) in social science for securing**99/100**.
- State rank **1st** in National science Olympiad in class X.

AREAS OF INTEREST

Hardware Neuromorphic computing platforms, Hardware security primitives, Novel Device Architectures for Sub-10 nm Regime, Analytical and Compact Modeling of Semiconductor Devices and Non-volatile Memories, Spintronics and Bio-Electromagnetics.

BOOK PUBLICATION

1. **Shubham Sahay** and M. Jagadesh Kumar, "Junctionless Field Effect Transistors: Design, Modelling and Simulation", ***Wiley-IEEE press, NJ, USA,*** ISBN: 978-1-119-52353-6,496 pages, Feb. 2019[click here].

JOURNAL PUBLICATIONS

Hardware Security Primitives

1. **Shubham Sahay**, M. Klachko, and Dmitri Strukov, "Hardware Security Primitive Exploiting Intrinsic Variability in Analog Behavior of 3-D NAND Flash Memory Array," ***IEEE Transactions on Electron Devices***, vol. 66, no. 5, pp. 2158-2164, May 2019. [click here] (*Impact factor:**2.7***)
2. **ShubhamSahay,** A. Kumar, V. Parmar, and Manan Suri, "OxRAM RNG circuits exploiting multiple undesirable nanoscale phenomena," ***IEEE Transactions on Nanotechnology***, vol. 16, no. 4, pp. 560-566, July 2017.(Appeared in the list of most popular papers in the month of January (amongst **Top 4**) 2017)[click here] (*Impact factor:**2.292***)
3. **Shubham Sahay** and Manan Suri, "Recent Trends in Hardware Security Exploiting Hybrid CMOS-NVM Circuits", ***IOP Semiconductor Science and Technology***, vol. 32, no. 12, pp. 123001, Oct2017. [click here](*Impact factor:**2.654***)

Mixed-Signal Neuromorphic Computing

4. **Shubham Sahay**, M. Bavandpour, M. R. Mahmoodiand Dmitri Strukov, "Energy-Efficient Moderate Precision Time-Domain Mixed-Signal Vector-by-Matrix Multiplier Exploiting 1T-1R Array," accepted for publication in ***IEEE Journal on Exploratory Solid-State Computational Devices and Circuits***.
5. **Shubham Sahay***, M. Bavandpour*, M. R. Mahmoodiand Dmitri Strukov, "Efficient Mixed-Signal Neurocomputing Via Successive Integration and Division," ***IEEE Transactions on VLSI systems***, vol. 28, no. 3, pp. 823-827, Mar. 2020. [click here] (*Impact factor:**1.95***)
6. M. Bavandpour, **Shubham Sahay**, M. R. Mahmoodi and Dmitri Strukov, "3D-aCortex: An Ultra-Compact Energy-Efficient Neurocomputing Platform Based on Commercial 3D-NAND Flash Memories" under review in ***IEEE Journal on Exploratory Solid-State Computational Devices and Circuits***. (major revision).

Compact Modelling

7. **Shubham Sahay**, and Dmitri Strukov, "A Behavioral Compact Model for Static Characteristics of 3D NAND Flash Memory," ***IEEE Electron Device Letters***, vol. 40, no. 4, pp. 558-561, April 2019. [click here] (*Impact factor:**3.753***)

Junctionless FETs

8. **Shubham Sahay** and M. Jagadesh Kumar, "Nanotube Junctionless Field Effect Transistor: Proposal, Design and Investigation", ***IEEE Transactions on Electron Devices***, vol. 64, no. 4, pp. 1851-1856, Apr. 2017.(Appeared in the list of most popular papers in the month of March, April and August 2017) [click here] (*Impact factor:**2.7***)
9. **Shubham Sahay** and M. Jagadesh Kumar, "Diameter Dependency of Leakage Current in Nanowire Junctionless Field Effect Transistors", ***IEEE Transactions on Electron Devices***, vol. 64, no. 3, pp. 1330-1335, Mar. 2017. (Appeared in the list of most popular papers in the month of January, February and April 2017)[click here] (*Impact factor:**2.7***)
10. **Shubham Sahay** and M. Jagadesh Kumar, "Insight into Lateral Band-to-Band-Tunneling in Nanowire Junctionless Field Effect Transistors", ***IEEE Transactions on Electron Devices***, vol. 63, no. 10, pp. 4138–4142, Oct. 2016. (Appeared in the list of most popular papers in the month of September (amongst **Top 5**) and November 2016) [click here] (*Impact factor:**2.7***)
11. **Shubham Sahay** and M. Jagadesh Kumar, "Controlling L-BTBT and Volume Depletion in Nanowire JLFETs Using Core-Shell Architecture", ***IEEE Transactions on Electron Devices***,vol. 63, no. 9, pp. 3790–3794, Sep. 2016.(Appeared in the list of most popular papers in the month of August (amongst **Top 4**) and September 2016)[click here](*Impact factor:**2.7***)
12. **Shubham Sahay** and M. Jagadesh Kumar, "Symmetric Operation in an Extended Back Gate JLFET for Scaling to the 5 nm Regime Considering Quantum Confinement Effects", ***IEEE Transactions on Electron Devices***, vol. 64, no. 1, pp. 21-27, Jan. 2017.(Appeared in the list of most popular papers in the month of January 2017)[click here] (*Impact factor:**2.7***)
13. M. Jagadesh Kumar and **Shubham Sahay**, "Controlling BTBT Induced Parasitic BJT Action in Junctionless FETs using a Hybrid Channel", ***IEEE Transactions on Electron Devices***, vol. 63, no. 8, pp. 3350-3353, Aug 2016. (Appeared in the list of most popular papers in the month of June, July and August 2016)[click here](*Impact factor:**2.7***)

14. **Shubham Sahay** and M. Jagadesh Kumar, "Realizing Efficient Volume Depletion in SOI Junctionless FETs", ***IEEE Journal of the Electron Devices Society***, vol. 4, no. 3, pp. 110-115, May 2016. (Appeared in the list of most popular papers in the month of February, March, April, May, June, July, August, September and November 2016) [click here] (*Impact factor:**2.0***)

Nanowire and Nanotube FETs

15. **Shubham Sahay** and M. Jagadesh Kumar, "Comprehensive Analysis of Gate-Induced Drain Leakage in Emerging FET Architectures: Nanotube FETs vs. Nanowire FETs",***IEEE Access,*** vol. 5, pp. 18918-18926 Dec. 2017.[click here] (*Impact factor:**4.1***)
16. **Shubham Sahay** and M. Jagadesh Kumar, "Spacer Design Guidelines for Nanowire FETs from Gate Induced Drain Leakage Perspective", ***IEEE Transactions on Electron Devices***, vol. 64, no. 7, pp. 3007-3015, July 2017**.** [click here] (*Impact factor:**2.7***)
17. **Shubham Sahay** and M. Jagadesh Kumar, "Physical Insights into the Nature of Gate Induced Drain Leakage in Ultra-Short Channel Nanowire Field Effect Transistors",***IEEE Transactions on Electron Devices,*** vol. 64, no. 6, pp. 2604-2610, June 2017.(Appeared in the list of most popular papers in the month of April, July, August and September 2017 and January, February, April (amongst **top 10**), May (amongst **top 10**), June (amongst **top 3**) andJuly 2018)[click here] (*Impact factor:**2.7***)
18. **Shubham Sahay** and M. Jagadesh Kumar, "A Novel Gate-Stack-Engineered Nanowire FET for Scaling to the Sub-10-nm Regime", ***IEEE Transactions on Electron Devices***,vol. 63, no. 12, pp. 5055-5059, Dec. 2016. (Appeared in the list of most popular papers in the month of November and December 2016) [click here] (*Impact factor:**2.7***)
19. A. K. Jain, **Shubham Sahay** and M. Jagadesh Kumar, " Controlling L-BTBT in Emerging Nanotube FETs using Dual-Material gate ", ***IEEE Journal of the Electron Devices Society***, vol. 6, pp. 611-621, June 2018. (Appeared in the list of most popular papers in the month of April, May and June 2018) [click here](*Impact factor:**2.0***)

Steep Switching FETs

20. G. Musalgaonkar, **Shubham Sahay**, R. S.Saxena, and M. JagadeshKumar, "A Line Tunneling Field-Effect Transistor Based on Misaligned Core-Shell Gate Architecture in Emerging Nanotube FETs," ***IEEE Transactions on Electron Devices***, vol. 66, no. 6, pp. 2809-2816, June 2019.[click here] (*Impact factor:**2.7***)
21. G. Musalgaonkar, **Shubham Sahay**, R. S.Saxena, and M. JagadeshKumar, "An Impact Ionization MOSFET with Reduced Breakdown Voltage Based on Back-Gate Misalignment," ***IEEE Transactions on Electron Devices***, vol. 66, no. 2, pp.868-875, Feb 2019.(Appeared in the list of most popular papers in the month of February 2019) [click here] (*Impact factor:**2.7***)
22. **Shubham Sahay** and M. Jagadesh Kumar, "Controlling the Drain Side Tunneling Width to Reduce Ambipolar Current in Tunnel FETs Using Hetero-dielectric BOX " ***IEEE Transactions on Electron Devices***, Vol. 62, no. 11, pp. 3882-3886, Nov 2015. (Appeared in the list of most popular papers in the month of November and December 2015) [click here](*Impact factor:**2.7***)
23. G. Musalgaonkar, **Shubham Sahay**, R. S.Saxena, and M. JagadeshKumar, "Nanotube Tunneling FET with a Core Source for Ultra-Steep Subthreshold Swing: A Simulation Study," accepted for publication in ***IEEE Transactions on Electron Devices.*** (*Impact factor:**2.7***)
24. G. Musalgaonkar, **Shubham Sahay**, R. S.Saxena, and M. JagadeshKumar, "An In-Line Tunnel Field Effect Transistor Based onInduced Channel for Improved Drive Current and Area Benefits," under review in ***IEEE Transactions on Electron Devices.***
25. **Shubham Sahay** and M. Jagadesh Kumar, "Ambipolar behaviour of silicon-on-thin-BOX (SOTB) tunnel FETs", ***IEEE Journal of the Electron Devices Society***. (Major revision).

Power MOSFETs

26. N. K. Saini, **Shubham Sahay,** R. S. Saxena and M. Jagadesh Kumar, "$In_{0.53}Ga_{0.47}As$/InP Trench Gate Power MOSFET based on impact ionization for improved performance: Design and Analysis", ***IEEE Transactions on Electron Devices,*** vol. 34, no. 11, pp. 4561-4567, Nov. 2017.[click here](*Impact factor:**2.7***)

CONFERENCE PUBLICATIONS

Hardware Security Primitives

1. **Shubham Sahay,** M. Suri, A. Kumar and V.Parmar, "Hybrid CMOS-OxRAM RNG circuits", ***IEEE NANO*** - *16th International Conference on Nanotechnology, Sendai, Japan,* Aug 2016. [click here]
2. A. Kumar, **Shubham Sahay** and M. Suri, "Switching-Time Dependent PUF Using STT-MRAM," *IEEE VLSI-D 17th International Conference on Embedded systems and 31st International Conference on VLSI Design*, 2018.[click here]

Mixed-Signal Neuromorphic Computing

3. **Shubham Sahay**, M. Bavandpour, M. R. Mahmoodi and Dmitri Strukov, "A 2T-1R Cell Array with High Dynamic Range for Mismatch-Robust and Efficient Neurocomputing," *IEEE International Memory Workshop* (**IMW**), 2020.
4. M. Bavandpour, **Shubham Sahay**, M. R. Mahmoodi and Dmitri Strukov, "Mixed-Signal Vector-by-Matrix Multiplication Circuits based on 3D-NAND Memories for Neurocomputing," *Design, Automation and Test Conference* (**DATE**), 2020.
5. M. Bavandpour, **Shubham Sahay**, M. R. Mahmoodi and Dmitri Strukov, "Mixed-Signal Neuromorphic Processors: Quo Vadis?," in *IEEE SOI-3D-Subthreshold (S3S) Microelectronics Technology Unified Conference*, 2019. (**Best paper nomination**)
6. **Shubham Sahay**, M. Bavandpour and Dmitri Strukov, "Compact Modelling and Computing Applications of 3D NAND Flash Memory," in *SRC TECHCON*, 2019.

PATENTS

1. Time-Domain Mixed-Signal Vector-by-Matrix Multiplier Exploiting 1T-1R Array, **US Patent.** (provisional application filed with M. Bavandpour and Dmitri Strukov, UC Case No. 2019-426).[click here]
2. Neurocomputing Platform Based on Commercial 3D-NAND Flash Memories, **US Patent.** (provisional application filed with M. Bavandpour, M. R. Mahmoodi and Dmitri Strukov, UC-2019-425). [click here]
3. Efficient Mixed-Signal Neuromorphic Computing via Successive Integration and Division, **US Patent.** (provisional application filed with M. Bavandpour, M. R. Mahmoodi and Dmitri Strukov, UC Case No. 2020-053).
4. Hardware Security Primitive Exploiting Intrinsic Variability in Analog Behavior of 3D NAND Flash Memory Array, **US Patent.** (provisional application filed with Dmitri Strukov, UC Case No 2019-401)

PROJECTS

Post-doctoral Research – University of California, Santa Barbara **(July 2018 –March 2020)**
Supervisor – Prof. Dmitri Strukov
Title–Development, Modeling and Characterization of Neuromorphic and Hardware Security Circuits based on Floating Gate Memories and Memristors.
Description –The emerging mobile devices in this era of internet-of-things (IoT) require a dedicated processor to enable computationally intensive applications such as neuromorphic computing and signal processing. Even the most advanced digital CPUs and GPUs are power inefficientowing to the inherent von Neumann architecture. Moreover, ultra-low power and compact hardware security primitives are essential in the functional circuits of the interconnected devices in the IoT ecosystem for protection against security vulnerabilities and adversary attacks. The relatively mature 3D NAND flash and emerging non-volatile memories (eNVMs) exhibit promising properties which may be exploited for ultra-low power in-memory computing and hardware security.

(a) Since 3D NAND flash memory has already become an integral part of the cyber-physical systems to cope with the huge data explosion,we develop the first behavioral compact model of 3D NAND flash memory to equip the circuit designers and system architects with an effective tool for its design-exploration for diverse unconventional analog applications.
(b) We propose an extremely dense, energy-efficient mixed-signal vector-by-matrix-multiplication (VMM) circuit based on the existing 3D-NAND flash memory blocks, without any need for their modification. We also propose 3D-aCortex, a multi-purpose neuromorphic inference processor that utilizes the proposed 3D-VMM blocks as its core processing units.
(c) We propose a physical unclonable function (PUF) exploiting the intrinsic variability in the string current of the ubiquitous 3D NAND flash memory owing to the process variations and the inherent material imperfections.
(d) We propose atime-domain mixed-signal VMM exploiting a modified configuration of 1 MOSFET-1 memristor (1T-1R) array which overcomes the energy inefficiency of the current-mode VMM approaches based on eNVMs.
(e) We propose a successive integration and division scheme to mitigate the challenges faced by the conventional time-domain VMM approaches.

PhD. Thesis – IIT Delhi **(July 2014 – November 2017)**
Supervisor – Prof. MamidalaJagadesh Kumar
Title–Design and Analysis of Emerging NanoscaleJunctionlessFETsfrom Gate-Induced Drain Leakage Perspective
Description–The thesis addresses the important issue of GIDL in emerging nano-scale FETs which increases the OFF-state leakage current in NWFETs and JLFETs and restricts the utility of TFETs for digital circuit applications. First, a physical insight into the nature of GIDL in different NWFET configurations is provided. The unforeseen impact of quantum confinement effects on the NWFETs is also revealed. A parasitic BJT theory is proposed to explain the difference in the nature of NWJLFETs and NWMOSFETs. The diameter dependent dominant leakage mechanisms in the NWJLFETs are then analyzed. A comprehensive analysis of GIDL in the recently reported nanotube (NT) FETs which are essentially NWFETs with a core gate is performed. A NTJLFET is also proposed to suppress the GIDL i.e. BTBT induced parasitic BJT action.

Furthermore, a NWFET with a dual metal stacked gate architecture (DMSG) is proposed to mitigate the GIDL and efficiently scale the NWFETs to the sub-10 nm regime. A core-shell NWJLFET with a p^+-core is proposed to (a) mitigate the BTBT induced parasitic BJT action in NWJLFETs with nanowire diameter < 10 nm and (b) realize efficient volume depletion in NWJLFETs with nanowire diameter >10 nm.The spacer design guidelines for: (a) NWFETs without source/drain extension underlap and (b) NWFETs with source/drain extension underlap are provided from a GIDL perspective. The efficacy of the dual-material gate (DMG) architecture to mitigate the GIDL in NWJAMFETs is also analyzed for the first time. An extended back gate architecture for scaling the double gate (DG) JLFETs to the sub-10 nm regime by diminishing the GIDL is proposed. In addition, a SOI JLFET with a hole sink layer to suppress the parasitic BJT action GIDL is presented. Buried oxide (BOX) engineering i.e. inclusion of a high-k BOX to realize efficient volume depletion and a hetero-dielectric BOX to mitigate the GIDL is also proposed for SOI JLFETs.
Back-gate engineering by utilizing a hetero-dielectric BOX and a modified ground plane in a silicon-on-thin-BOX (SOTB) TFET are proposed to suppress the ambipolar conduction (GIDL) in TFETs.

Hybrid CMOS-RRAM circuits for IoT Security– Course Project, Non-volatile memory, IIT Delhi (July 2015 – Dec 2015)
Supervisor – Prof. Manan Suri
Description –(a)Proposed a scalable and power efficient random number generator (RNG) circuit exploiting the *reset* state transient current fluctuations of the Ox-RAM devices. Two different hybrid circuits were proposed: a pseudo-random number generator (PRNG) utilizing a single Ox-RAM device and a True RNG (TRNG) circuit with two Ox-RAM devices coupled to the source/drain terminals of a MOSFET. (b) A physically unclonable function (PUF) based on the time dependent probabilistic switching in STT-MRAM was also proposed. (c) Invited by IoP Semiconductor Science and Technology journal as a leading authority in this field to write a topical review on Hybrid CMOS-RRAM circuits for IoT security.

INUP hands-on-fabrication workshop – CeNSE, IISc Bengaluru (Feb 2018 – March 2018)
Description –Completed hands-on-fabrication training at Centre for Nano Science and Engineering (CeNSE) at IISc, Bengaluru. Hands-on experience with mechanical, optical and material measurement techniques such as SAM for defects, optical profilometer, UTM for measuring stress, SEM, FIB, TEM, Raman, PL, XRD, STA and FT-IR spectroscopy.
Tools used: oxidation and diffusion furnace, RTP, LPCVD.
Inline characterisation facilities such as ellipsometer and Dektak surface profilometerand KMOS ultra scan for stress.
Thin film deposition using PVD, DC/RF sputtering, PECVD and ALD.
E-beam lithography and optical lithography
Dry etching techniques such as plasma etching, physical sputtering, RIE and DRIE.
Fabricated a MOS capacitor and submitted a project proposal for fabrication of a Junctionless FET.

Neuromorphic computing using spintronics – IIT Delhi (Jan 2017 – July 2017)
Supervisor – Prof. DebanjanBhowmik
Description –Implementation of an ultra-low power all-spin neuromorphic computing system utilizing skyrmion motion using mircromagnetic simulations.

B.Tech Project (part II) – IIT BHU (Jan 2014 – Apr 2014)
Supervisor – Prof. SatyabrataJit
Title –Analytical Modeling and Simulation of Linearly Graded Gate Workfunction FD-SOI MOSFET
Description – Simulated and developed an analytical model for the FD-SOI MOSFET with a gate having a work function which reduces linearly from the source-channel interface to the drain-channel interface. The MOSFET with a linearly graded work function exhibits a higher mobility and a lower short channel effects compared to the conventional FD-SOI MOSFETs. The model for surface potential and threshold voltage was developed by solving the 2D Poisson's equation using appropriate boundary conditions.

B.Tech Project (part I) – IIT BHU (Aug 2013 – Nov 2013)
Supervisor – Prof. SatyabrataJit
Title –Analysis of FD-SOI MOSFET with LDD and highly doped GP back gate.
Description – Simulated FD-SOI MOSFET with a lightly doped drain for reduced short channel effects and investigated the impact of ground plane doping on the characteristics of the FD-SOI MOSFETs. The effect of BOX thickness, the GP doping and the LDD doping was extensively studied.

Summer Internship –WESEE, INDIAN NAVY Headquarter, Ministry of Defence, New Delhi. (May 2013 – Jul 2013)
Supervisor – Hemant Garg (Scientist "E", DRDO)
Title –Equalizer algorithms for reliable ship to ship communication
Description – Simulated the entire ship to ship communication system in MATLAB by modeling the medium as a Rayleigh channel and implemented various equalizer algorithms to reduce the inter-symbol interference (ISI). The different equalizer algorithms such as the zero forcing algorithm, least mean square (LMS), recursive least mean square (RLS) and adaptive algorithms were compared using the bit error rate as the figure of merit.

PROFFESIONAL COURSES

PG Level Courses:
Microelectronics,
Solid State Devices,
Compact Modeling,
Non-volatile Memories and Neuromorphic Computing,
IC Fabrication Technology,
MOS VLSI,
Analog Circuits,
Microwave Solid State Devices,
MEMS,
Digital Signal Processing,
CAD of VLSI,
VLSI Labs – Circuit Design and Layout,
Physical Design Lab: Frontend and Backend Digital Design

UG Level Courses:
Microwave Communication Systems
Satellite Communication,
Switching Theory and Finite Automata,
Radar Engineering,
LSI and VLSI Design,
Optical Communication,
Industrial Sociology,
Industrial Management,
Reliability Engineering,
Logic Design of Switching Circuits,
Control Systems,
Computer Architecture,
Power Electronics,
Microprocessor Engineering,
Control Systems Analysis,
Microwave Engineering,
Electronic Measurements and Instrumentation,
Materials Science,
Antennas and Wave Propagation,
Analog circuits and systems,
Analog communication,
Signals and Systems,
Network Analysis and Synthesis,
Electromagnetic Theory,
Electrical Engineering Labs – Circuits and Machine Labs
Analog and Digital circuits Lab
Analog and Digital communication Lab
Microwave Engg. Lab
Microprocessor Lab
Microelectronics Lab
Optical Communication Lab
CAD and DSP Lab

Mathematics: Courses covering real and complex analysis, linear algebra and differential equations, probability and statistics.
Physics: Courses covering mechanics, electrostatics, electrodynamics, wave theory, thermodynamics, and modern physics.
Chemistry: Courses covering basic physical, inorganic and organic chemistry.

TECHNICAL SKILLS

Programming Language: Python, C, C++, VHDL, Verilog and LINDO API.
Tools: TCAD Silvaco ATLAS, TCAD Sentaurus, Agilent ICCAP, MuMax3, MATLAB, Xilinx, Cadence Virtuoso, H-SPICE, Cadence Spectre, Cadence Encounter, Simulink, LINGO, Code Composer Studio, Proteus.
Hardware: Parameter analyzer (Agilent B1500A), FPGA boards, Microcontrollers, Function Generators, Microprocessors.

EXTRA CURRICULAR ACTIVITIES AND ACHIEVEMENTS

- Co-ordinator of FUNCKIT (circuit designing event) in AAYAM 2013, the departmental festival of Electronics Engg. atIIT BHU.
- **2nd** prize in ANALOCK (analog circuit designing) event held in AAYAM 2012,the departmental festival of Electronics Engg. atIIT BHU.
- **2nd** prize in I-ROBO (line follower robot) event held in TECHNEX 2011,the techno-management festival of IIT BHU.
- **1st** prize in the inter-year cricket tournament in 2013 and 2014 organized by the Electronics Engg. Society, IIT BHU.
- Pursued 6 years in vocal classical music with distinction every year from PrayagSangeetSamiti,Allahabad.
- Participated in Robosoccer (manually controlled robot which plays football) in TECHNEX 2011 and Optika (the image processing robot) event held in TECHNEX 2012.
- Participated in Sigpro (signal processing event) held in AAYAM 2012.
- **1st** prize in vocal music at state level in class X.
- Active member of the Robotics club at IIT BHU and mentored junior students for various events.
- Active member of Kashi-Utkarsh (social organisation of IIT BHU) which works for teaching kids in slum areas of Varanasi.
- Participated in the inter-hostel Cricket tournament of IIT Delhi from Udaigiri House team in 2016.
- Organised and performed Solo vocals in Teacher's day celebration of VLSI group, IIT Delhi in 2015, 2016 and 2017.

REFERENCES

Dr. M. Jagadesh Kumar
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Dr. Dmitri Strukov
Professor (Post-doc advisor)
Electrical and Computer Engineering,
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Dr. SatyabrataJit
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IIT (BHU) Varanasi
Email: sjit.ece@itbhu.ac.in