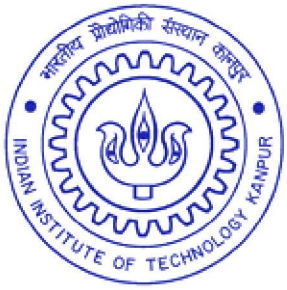
Optical Packet Switching Architectures Incorporating Various Buffering Techniques using Fiber Delay Lines

by

RAJAT KUMAR SINGH



DEPARTMENT OF ELECTRICAL ENGINEERING

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Optical Packet Switching Architectures Incorporating Various Buffering Techniques using Fiber Delay Lines

A *Thesis Submitted*

in Partial Fulfilment of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY

by

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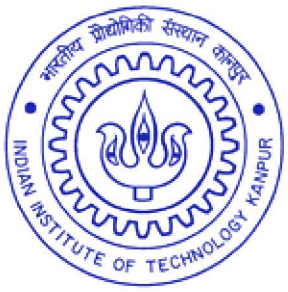

to the

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CERTIFICATE

It is certified that the work contained in the thesis entitled "**Optical Packet Switching Architectures Incorporating Various Buffering Techniques using Fiber Delay Lines**" being submitted by **Mr. Rajat Kumar Singh** has been carried out under my supervision. In my opinion, the thesis has reached the standard fulfilling the requirement of regulation of the Ph.D. degree. The results embodied in this thesis have not been submitted elsewhere for the award of any degree or diploma.

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13 May, 2007

Dedicated

to

my Grandfather

Acknowledgements

People prefer to follow those who help them,

not those who intimidate them.

— C. Gene Wilkes

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(Rajat Kumar Singh)

Synopsis

Name of the Student	:	**Rajat Kumar Singh**
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The bandwidth demand due to more and more data intensive applications and growth in userbase, is increasing day by day. Optical networks are the most suitable option for satisfying this increased bandwidth requirements, due to the availability of large bandwidth in the fiber [16, 68]. The optical network implementations can have electronic or all-optical switches. In optical transport networks, the current approach is to use optical circuit switches to set up light paths [1, 49, 59]. These all-optical switches are transparent to information carried over the light path. The possibility of packet switching using photonic technologies, allows all-optical packet switched networks where packets remain in optical form without undergoing optoelectronic conversion at intermediate nodes.

One of the major issues involved in optical networking is the switch/router architecture which can perform the switching operation efficiently at such high data rates.

The purpose of switching is to route the packet to the destined output port. The important aspects of photonic packet switching are control, packet synchronization, clock recovery, packet routing, contention resolution and packet header replacement [18, 64]. Contention is one of these problems, which occurs when two or more packets arrive at same time for same destination. To avoid this contention, one of the contending packets, is directed to the intended output port and other packets are either stored or dropped. All-optical memory suitable for optical storage has not yet been developed. The alternative is to use deflection routing [13] or optical fiber delay lines (in traveling or recirculating type configuration). Different techniques for optical buffering by using fiber delay lines have been proposed [7, 31, 32, 56], and still research is going on to explore better solutions. Optical buffering can be introduced in three ways: input buffering, output buffering and shared buffering [2, 6, 15, 29].

In this thesis, different aspects of optical buffering are investigated in various architectures for optical packet switching. Some new architectures have also been proposed alongwith the buffering techniques and their analysis. The main objective of the thesis, is to identify the optimal buffering parameters to provide least packet loss probability and reasonable average delay using the given resources.

The thesis is organized in the following nine chapters.

In **Chapter 1**, first we have explained the evolution of lightwave communication techniques. Then, we have given a review of related literature, providing a motivation to the study carried out in this thesis.

In **Chapter 2**, we have given the basic overview of the photonic packet switching architectures. We also discuss the switching/buffering technologies and the optical components used in the switch architectures.

Chapter 3 proposes a modification in the Staggering switch architecture [28], by adding the fiber delay line (FDL) to improve its performance. The effectiveness of modification, has also been discussed.

In **Chapter 4**, we have presented a new approach of switching in Data Vortex switch architecture [71] to improve its performance. Simulations have been done and the results are analyzed to find the advantages. Throughput analysis is also done, which is not performed so far.

In **Chapter 5**, we have proposed a new optical packet switch architecture which uses shared loop buffer modules in feedback configuration. WDM based fiber delay lines are used to store the contending packets, and a space switch fabric is used to direct them appropriately. These delay lines incorporate various optical components which induce loss in the signal power, during recirculation of signal in the loop. We have done the power budget analysis considering the effect of noise to calculate the number of maximum allowed circulations for a packet, in the loop buffer. The buffering duration in the recirculating loop, is limited by this circulation limit. The results for packet loss probability and average delay, are obtained using a specific scheduling algorithm and simulation techniques. The mathematical analysis has also been done to validate the simulation results.

Chapter 6 discusses about the enhancement in the optical packet switch architecture proposed in Chapter 5. The main disadvantage of this architecture, is very high loss in signal power, which reduces the number of maximum allowed circulations in loop buffer modules. Thus to reduce the power loss, we have proposed two modifications. The main objective of these modifications is to increase the number of maximum allowed circulations. This will provide a relaxation in the circulation limit, which in turn

results in better packet loss probability and average delay by effectively utilizing the available buffer capacity.

In **Chapter 7**, we have proposed three architectures for optical packet switching based on wavelength routed feed-forward shared buffer modules. These architectures are developed by selecting three different combinations of space switch and Arrayed Waveguide Grating (AWG). The buffer modules are constructed using recirculating type fiber delay lines incorporating various optical components. One of these architectures is also analyzed in terms of power loss and noise power, due to the presence of various optical components in loop buffer memory. The performance is predicted on the basis of operational insights. Further, the same has been verified by getting results for the packet loss probability and average delay by simulations.

Chapter 8 presents the comparative analysis of various optical packet switch architectures, discussed in the previous chapters. The comparison is done on the basis of optical cost of switch architectures and performance for bursty traffic arrival.

Finally, **Chapter 9** provides conclusion of the thesis, and suggestion for the future research in this area.

Contents

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List of Symbols

R	Responsivity
n_{sp}	Population inversion factor
h	Planck's Constant
B_e	Electrical Bandwidth
B_o	Optical Bandwidth
q	Electronic charge
ε	Extinction Ratio
R_L	Load Resistance
T	Temperature
K_B	Boltzmann constant
L_{3dB}	3dB coupler Loss
L_{Com}	Combiner Loss
L_{SP}	Splitter Loss
L_{DEMUX}	DEMUX Loss
L_{AWG}	Array Waveguide Grating Loss
L_{TWC}	TWC Loss
L_{FF}	Fixed Filter Loss
L_S	Splice Loss
$L_{F1} = L_{F2}$	Fiber Loss
L_S	Splice Loss
L_{BPF}	Band Pass Filter Loss
L_{SS}	Space Switch Loss
Γ	Confinement Factor
γ	Scattering Loss
P_p	Pump Power

List of Acronyms

AGC	Automatic Gain Control
ASE	Amplified Spontaneous Emission
ATM	Asynchronous Transfer Mode
AWG	Array Waveguide Grating
BER	Bit Error Rate
BL	Burst Length
BPF	Band Pass Filter
DEMUX	Demultiplexer
DWDM	Dense Wavelength Division Multiplexing
DXC	Digital Cross Connect
E/O	Electronic to Optical Conversion
EDF	Erbium Doped Fiber
EDFA	Erbium Doped Fiber Amplifier
FCC	Fiber-to-Chip Coupling
FCFS	First-Come-First-Serve
FDL	Fiber Delay Line
FF	Fixed Filter
FIFO	First-In-First-Out
ITU	International Telecommunication Union
IP	Input Pattern
IR	Injection Ratio
MSN	Manhattan Street Network
O/E	Optical to Electronic Conversion
OADM	Optical Add-Drop Multiplexer
OBS	Optical Burst Switching
OPS	Optical Packet Switching
OXC	Optical Cross Connect

RCP	Routing Control Processor
SNR	Signal to Noise Ratio
SOA	Semiconductor Optical Amplifier
TAG	Tell-and-Go
TDM	Time Division Multiplexing
TWC/TOWC	Tunable Wavelength Converter
WDM	Wavelength Division Multiplexing

Chapter 1

Introduction

The word telecommunications is made up of two words: *tele* (over a distance) and *communications* (exchange of information). Thus the exact meaning of telecommunication can be defined as the transmission of information over long distance using suitable equipments e.g., telephone. Most of the time, the information to be exchanged with others are voice, video and/or data. The information in these forms is transmitted using the transmitter. The transmitter processes the information appropriately (by multiplexing and/or modulating it) into the suitable format (electrical or optical signal) and then transmits it. The signal travels through communication links (transmission media) which can be copper wire, coaxial cable, optical fiber or free space. The intended receiver accepts this transmitted signal from the channel and processes it (by demodulating and/or demultiplexing it) to recover the information.

1.1 Evolution of Communication Techniques

In the first quarter of 19^{th} century, the evolution of electrical communication was led by the invention of telegraphy. Data transmission was done with rates up to 10b/s by the

application of coding techniques such as Morse code. Alexander Graham Bell invented the telephone in 1876 and the first telephone line ever, which ran between the second floor and the basement of Bell's house, was an example of what's today called a point-to-point link. That dedicated link gave birth to the modern telecommunications, and this technique has dominated the communication systems for almost a century. With the use of coaxial cable, the system capacity increased up to 100Mb/s in 1970s.

In the past (till 18^{th} century), the common method for transmission of information was fire and smoke signals as well as the reflecting mirror. Then some improvements had been done by the introduction of devices such as flags, signaling lamps or semaphores. Bell tried to send speech over a visible light beam in 1860 for distances of several hundred meters using photophones [4]. But these photophones were impractical because of the requirement of line of sight and the presence of the atmospheric disturbances such as rain, snow, fog, dust and turbulence. Maiman developed the laser in 1960 and this was the first production of coherent light [41]. The use of optical fiber based on silica glass as transmission medium had been proposed in 1966 [37]. These developments gave rise to the first generation of lightwave communication systems. The data rate achievable at that time was much better than that of electrical signal but still it was limited because of attenuation and dispersion in the fiber. In the initial phase, the fiber was operated at wavelength near $0.8\mu m$ due to the availability of cheaper silicon detector. In the second generation of lightwave systems, the laser and detectors were invented for operation at $1.3\mu m$ with attenuation of 0.35dB/km and produced the optical data at 2Gb/s in 1980s [69]. The third generation of fiber optics communications is functional at $1.55\mu m$ and 10Gb/s with attenuation of 0.2dB/km [22]. Simple optical communication links have been evolved to an extent where optical components and fibers are used to form the current fast growing optical networks.

1.2 Optical Networks

The bandwidth demand due to more and more data intensive applications is increasing day by day. Optical networks are the most suitable option for this increased bandwidth requirements due to the availability of large bandwidth in the fiber [16, 53, 68]. The optical network implementations can have electronic or all-optical switches. Electronic switches are easy to implement due to mature electronics technology but they have fundamental limitations on rates at which data can be transported from one switch to another switch. This limit is not because of communication channel (i.e., optical fiber) but due to modulation and demodulation limits in electronic transmitters and receivers respectively.

In optical transport networks, the current approach is to use optical circuit switches to set up light paths [1, 49, 59]. These all-optical switches are transparent to information carried over the light path. At the same time, optical circuit switching technology has made it feasible to have virtual topologies over an actual physical fiber topology (layout). It allows us to rapidly deliver the enormous bandwidth of WDM networks to the customer, while remaining inefficient at the physical layer. One requires packet switching for efficient use of the physical layer. The possibility of packet switching using photonic technologies allows all-optical packet switched networks where packets remain in optical form without undergoing optoelectronic conversion at intermediate nodes. Thus, photonic packet switching offers high speed (data rate), format transparency, efficiency and flexibility in configuration due to the switching operation in physical layer. Since the data is generated by electronic sources, the only motivation to build the all-optical packet switch is when ingress routers aggregate the large number of packets optically for very high bit rate payload. This can be attached with low bit rate

header and pushed into the core network. The all-optical packet switches in the core will convert the header of the packet to electrical form and keep the payload in optical form. The header information can be used to route the packet. Once the packet reaches the egress node, the aggregated packets can be separated optically and passed onto the client network [18, 19, 26, 33, 36, 48]. We can call them as aggregate core transport networks.

Wavelength division multiplexing (WDM) allows transmission of hundreds of channels in a single fiber where each channel may operate at the speed of 10Gbps to 40Gbps. Thus it increases the network capacity tremendously by harnessing the large available bandwidth of optical fiber, and it can also satisfy the ever increasing bandwidth demand [14, 17, 43, 46, 54].

1.3 Optical Packet Switching

One of the major issues involved in optical networking is the switch/router architecture which can perform the switching operation efficiently at such high data rates. In the last decade, several research works have been reported on the design of switches/routers. These switches are of various types: electronic, 'all'-optical or 'almost-all'-optical. The purpose of switching is to route the packet to the destined output port. The important aspects of photonic packet switching are control, packet synchronization, clock recovery, packet routing, contention resolution and packet header replacement [18, 64]. These are considered as the key issues for successful operation of an optical packet switch. Contention is one of these issues, which occurs when two or more packets arrive at the same time for the same destination. To avoid this contention, one of the contending packets is directed to the intended output port and other contending packets are either

stored or dropped. All-optical memory suitable for optical storage has not yet been developed. The alternative is to use deflection routing [13] or optical fiber delay lines (in traveling or recirculating type configuration). Different techniques for optical buffering by using fiber delay lines have been proposed [7, 28, 31, 32, 56, 65] and still, the research is going on to explore better solutions. Optical buffers are much better than the electronic buffers because in case of optical buffers, the data path is: i) all-optical i.e., O/E and E/O conversion not required, ii) having larger bandwidth, iii) data rate transparent and iv) capable of supporting WDM. Optical buffering can be introduced in three ways: input buffering, output buffering and shared buffering [2, 6, 15, 20, 29, 31, 56]. Shared buffer optical switches are more advantageous as compared to the other two categories because it also provides switching alongwith buffering. These shared type buffers can be implemented in the optical switches either in the feedback or in the feed-forward manner [12, 30, 40, 74]. Both of these configurations have their advantages and disadvantages, and are used as per the requirement of the switch architecture.

1.4 Outline of Thesis

In the thesis, different aspects of optical buffering are investigated for various architectures of optical packet switching. Some new architectures are also proposed alongwith the buffering techniques and their analysis. The main objective is to utilize the optimal buffering parameters to provide least packet loss probability and reasonable average delay with the given resources.

The rest of the thesis is organized in following manner. **Chapter 2** gives the basic overview of photonic packet switching architectures and the optical components used in these architectures. **Chapter 3** deals with the proposed modification in the architec-

ture of staggering switch to improve its performance. In **Chapter 4**, we present a new approach of switching for data vortex architecture. **Chapter 5** proposes a new optical packet switch architecture which uses loop buffer modules in feedback configuration. Power budget analysis is performed by taking care of various types of noise in the loop buffer module, and the number of maximum allowed circulations in the loop buffer is calculated. Mathematical analysis is also done to validate the simulation results as well as the proposed architecture. **Chapter 6** discusses enhancements to the optical packet switch architecture proposed in Chapter 5. The main objective of these enhancements is to increase the number of maximum allowed circulations. In **Chapter 7**, we propose three architectures for optical packet switching based on wavelength routed feed-forward shared buffer modules. These architectures are developed by selecting three different combinations of space switch and Arrayed Waveguide Grating (AWG). One of these architectures is also analyzed in terms of power loss and noise power, due to the presence of various optical components in the loop buffer memory. **Chapter 8** presents the comparative analysis of various optical packet switch architectures (discussed in the previous chapters), on the basis of optical cost and bursty traffic arrival. Finally, **Chapter 9** concludes the thesis alongwith some suggested future works.

Chapter 2

Photonic Packet Switching Architectures - A Literature Survey

In this chapter, we briefly discuss the issues related to photonic packet switching and their architectures[1]. We will also give a brief detail of few optical components which are commonly used in various switch architectures of the following chapters.

2.1 Electronic Packet Switching Technologies

The goals of a packet switching system are high throughput, low latency, low packet loss and effective prioritized processing. At the architectural level, several parameters need to be chosen/rejected before converging onto a suitable design. Some of these parameters are switching fabric structure, buffering and queuing strategy, scheduling algorithm and flow control. Basic switching fabric can be of different sizes depending upon several constraints such as maximum permitted blocking probability. One can configure the switching fabric in the form of either a large element in single stage or

[1] "An overview of photonic packet switching architectures," *IETE Tech. Rev.*, Vol. 23, No. 1, pp. 15-34, 2006.

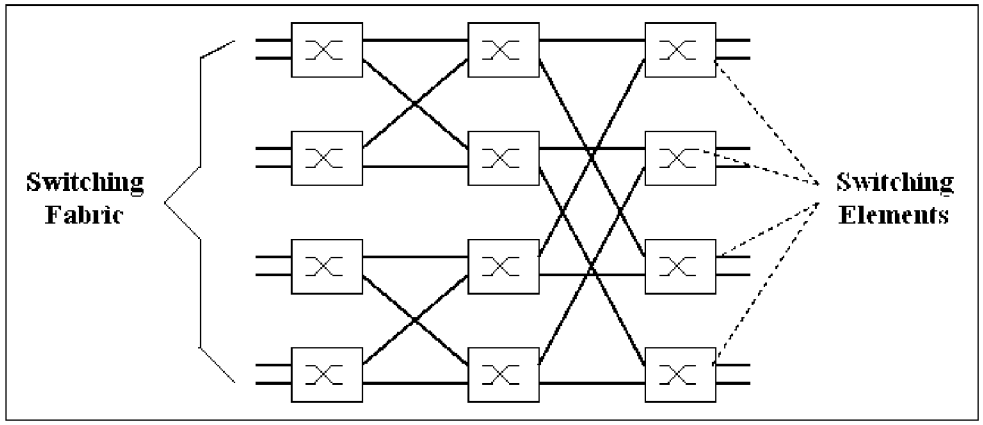


Figure 2.1: Multi-stage Interconnection Network

several small elements in multiple stages. Multistage interconnection networks e.g., Clos network and Banyan network (Figure 2.1), can be used for configuring larger switches using smaller ones [34].

Multiple packets arriving at the same time from different input ports may be destined to the same output port, and will cause contention for that output port. In this condition, one of the contending packets will be passed to the destination and the rest of the contending packets will be stored, if possible, in the buffers to avoid the loss of packets. These buffered packets are queued using an appropriate algorithm and delivered to the designated output port in later free time slots. These buffers can be placed at different locations in the switch [70] and depending upon the placement, buffering can be classified as Input buffering (Figure 2.2), Output buffering (Figure 2.3) and Shared buffering (Figure 2.4).

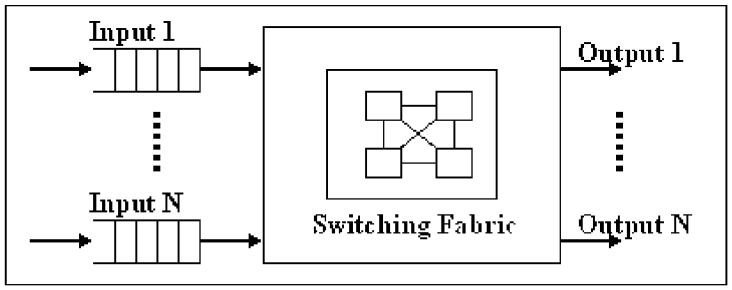


Figure 2.2: Input buffering arrangement

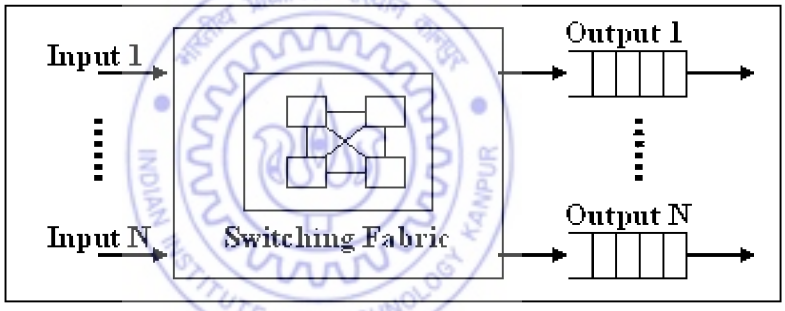


Figure 2.3: Output buffering arrangement

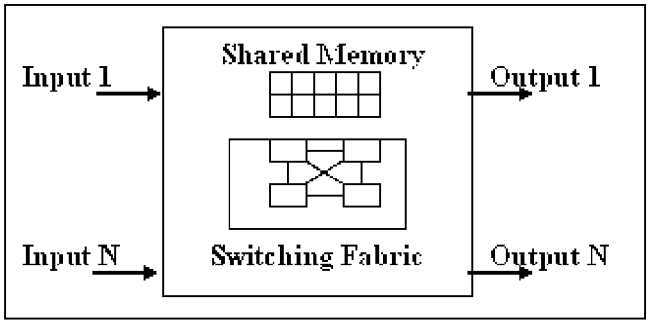


Figure 2.4: Shared buffering arrangement

2.2 Optical Packet Switching Technologies

Optical packet switching can be categorized as 'almost-all' and 'all' optical switching. In both types, the data path is fully optical, but they differ in control functionality. In 'almost-all' optical switching, the control of switching operation is done electronically while in 'all' optical switching, the control is expected to be fully optical or optoelectronic. Optical packet switching can be further subdivided into (a) Photonic Packet Switching, and (b) Optical Burst Switching.

2.2.1 Photonic Packet Switching

Photonic packet switching combines high capacity of optical links as well as fine granularity and efficient multiplexing of packet switching. The wide bandwidth of photonic components, combined with the flexibility of WDM and the high speed capabilities of optical devices, provides the potential for building packet switched networks with throughputs in the range of terabits per second (Tbps) [64, 72]. Some of the critical issues involved in designing and implementing photonic packet switches are:

1. Switch Architecture,
2. Header and packet format,
3. Routing Strategies,
4. Contention Resolution and Switching,
5. Synchronization, and
6. Header Regeneration.

2.2.1.1 Switch Architecture

Photonic packet switches can be modelled in terms of the constituent subsystem (Figure 2.5) i.e., the photonic switch fabric, the routing control processor (RCP) and the input & output interface units [7]. The switch fabric creates optical connection between input and output, which may be one-to-one, one-to-many or many-to-one. The RCP sets the connection state of the switch, while taking care of internal blocking state and output port contentions. Several photonic packet switch architectures have been proposed, and all of them use photonic means to perform packet buffering and routing; while electronics is used for address processing, routing and buffering controls [64].

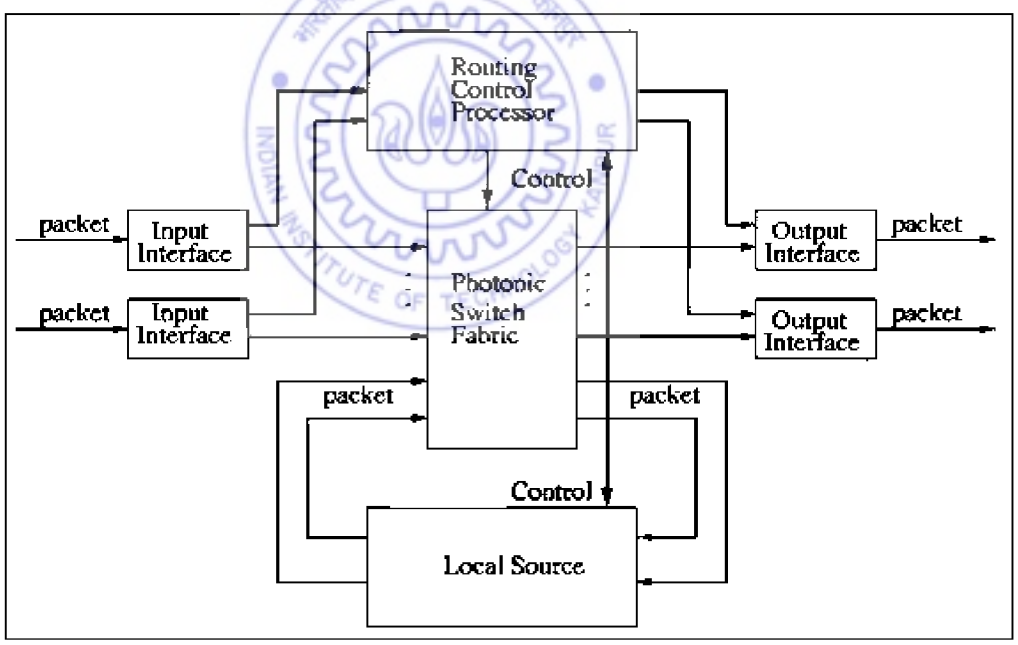


Figure 2.5: General Architecture of Photonic Packet Switch

These switch architectures are classified in the following ways:

(a). Space-Switch based Photonic Packet Switch: A space division switch simply provides the ways for the transmission of packets from inputs to the respective

outputs. For an example, space switches can be implemented using semiconductor optical amplifiers (SOA) as the basic transmission gate. An $N \times N$ space-switch based on SOA gate is shown in Figure 2.6. It consists of N splitters of $1 \times N$ size, N^2 SOA gates and N combiners of $N \times 1$ size. Each input i split to N gates and if the signal at that input is to be switched to output j, then the j^{th} gate is switched to ON state and all others are kept in OFF state.

In the context of photonic packet switching, optical space switches are required to have a switching speed in the range of several nanoseconds as the switching time has to be less than 10% of a packet time to achieve a high utilization in transmission. Further, low crosstalk and low power loss is desirable. The staggering switch [28] (described in chapter 3) is an example of space switching based optical packet switch. It uses space switches to perform packet routing and buffering.

(b). Broadcast-and-Select Packet Switch: In this approach, information from all the signal sources is multiplexed by a star coupler and distributed to all the receivers where each receiver selects the desired packets. Both TDM and WDM can be used in this approach. An example of this type of switch is shown in Figure 2.7. It consists of N tunable wavelength converters at the input, a random wavelength accessible recirculating loop buffer, and N tunable filters at the output [5]. The loop buffer is shared by all the packets from all the inputs. Before entering the buffer, each packet is assigned a wavelength not being used by any other packet within the buffer. All the packets in the buffer are broadcast to all the outputs. The tunable filter at each output selects appropriate packets by tuning its transmission wavelength. The packets which are selected by the tunable filters are cleared out of the buffer by turning off the corresponding gate switches in the buffer. An electronic controller tracks N packet queues corresponding to N outputs of the switch.

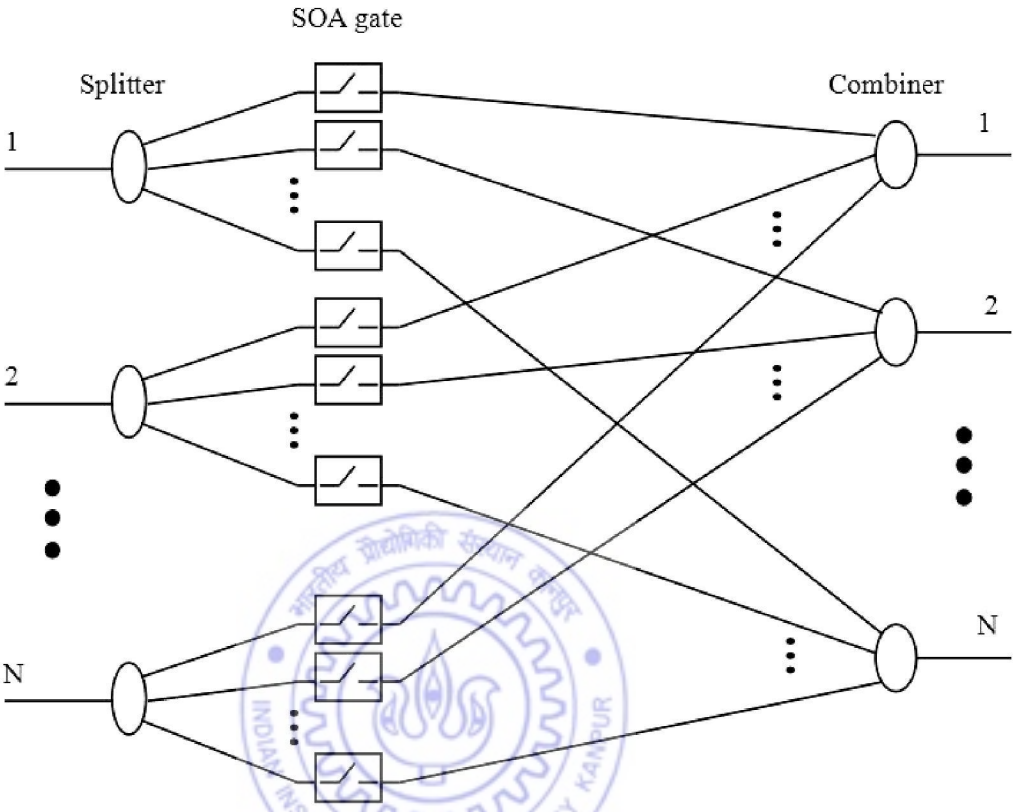


Figure 2.6: SOA gate based space division switch

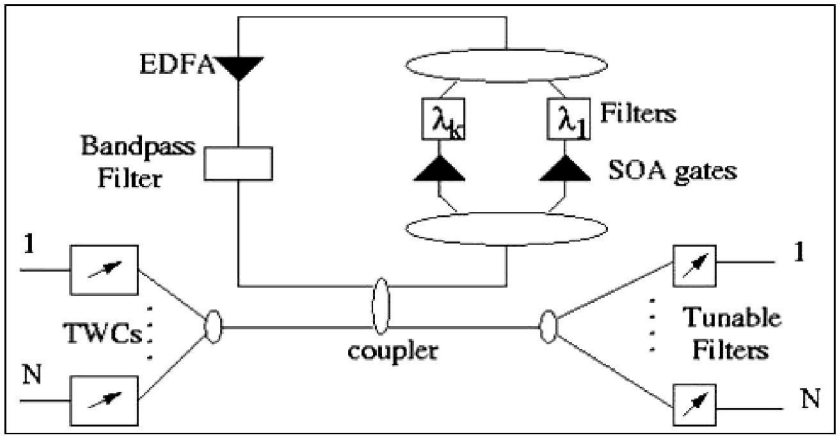


Figure 2.7: Broadcast-and-select photonic packet switch

(c). Wavelength-Routed Photonic Packet Switch: This type of packet switch uses wavelength coding for packet routing and buffering. An example is shown in Figure 2.8. It consists of three functional blocks: a packet encoding block, a buffering block and a packet demultiplexing block [64]. The packet encoding block comprises of N optical tunable wavelength converters (TWCs), and each of these convert the incoming packets to the wavelength corresponding to its desired output i.e., a packet addressed to the i^{th} output is assigned a wavelength λ_i. The buffering block consists of an $N \times K$ SOA gate switch matrix followed by a set of K optical delay lines whose lengths range from 0 to $(K-1)$ packet times. The wavelength encoded packets are provided access to appropriate delay lines using SOA gate switch matrix. This is done in such a way that the packets, destined for a given output, leave the switch following the first in first out (FIFO) scheme. FIFO is a queuing discipline where the packet entering earlier in the queue for an output is always sent to that output, earlier than all the packets arriving later.

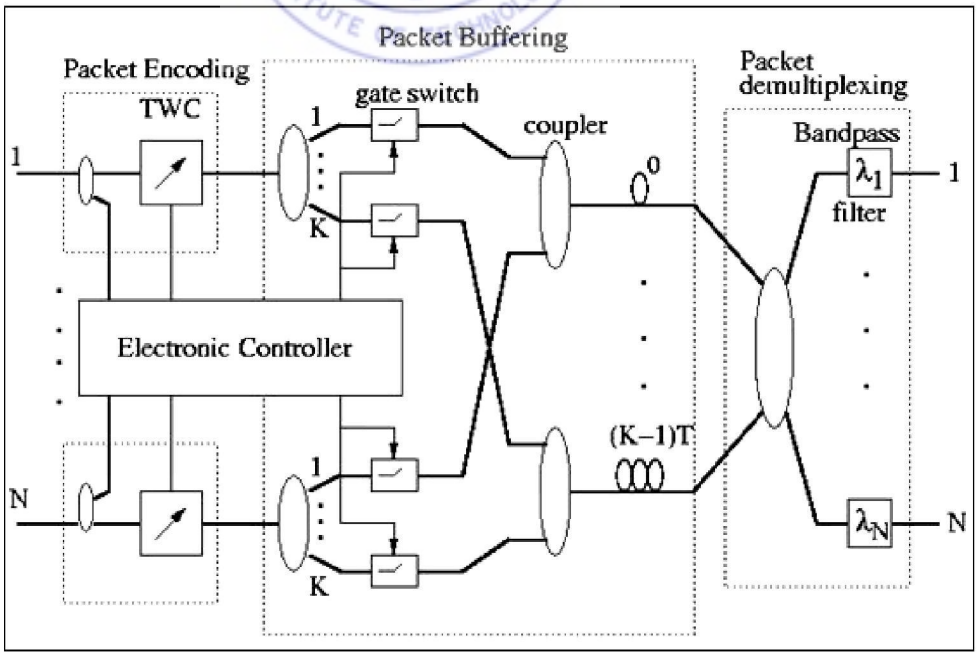


Figure 2.8: Wavelength routed photonic packet switch

The demultiplexing block consists of a $K \times N$ star coupler followed by a set of N bandpass filters, one at each output to select packets whose wavelengths matches with its passband. An electronic controller is used to control the TWCs and space switches to implement the switching function. In this architecture, the number of SOA gates required in the buffering blocks increases proportionally to the product of N and K. Also, the optical power loss of a packet is proportional to NK^2 (for $N < K$) or N^2K (for $N > K$). This limits the scalability of the switch.

2.2.1.2 Header and packet format

A packet can be functionally described using a layered model. At the physical level, there are effectively two such layers: the header and the payload. The *header* contains information processed only by the switches. It may include destination address, priority, packet empty-full bit and packet length. The *payload* contains information processed only by the sources and destinations. It may include data, packet number and source address.

In electronic networks, routers or switches will process the header information arriving at the same data rate as the payload. In an N port switch, the control processor should be able to process on an average $N \times L$ headers in a slot duration. Here, L is the maximum loading per line for which, that switch is designed. This will ensure that no packet is dropped because of the unprocessed header. In an optical network, the bandwidth is much larger than their electronic counterpart and hence, the slot duration for packets will also be small. As a consequence the number of headers which can be processed in a slot time, reduces drastically for the same processor thereby limiting the switch size. Alternatives to resolve this problem are as follows: i) to use larger packet size and hence larger slot size or ii) for smaller slot size, use smaller size switches with

their own processors and interconnect them to make a large switching network; this is distributed switch or iii) make the header format simple enough for faster processing.

In the literature [7], three basic categories for optical packet coding have been proposed to make the header processing faster. These are *bit-serial*, *out-of-band-signaling*, and *bit-parallel*. Each of these techniques exploit the data rate and format transparency of optical devices. These techniques are well described in [7, 59] alongwith their comparative analysis.

2.2.1.3 Routing Strategies

Routing is the mechanism which chooses a preferred path to send a packet from its source to destination. Routing control is a mechanism which configures the paths in switches to facilitate the movement of a packet to the next chosen switch. It may be centralized or distributed. *Centralized control* involves a single processor monitoring the network and setting up the switch state according to the routing request. But, as the networks become large or incorporate more switches, centralized control increases latency, degrades throughput, and also increases processing complexity. In *Distributed control*, packets carry destination information for independent processing at each node. This form of processing reduces the burden on a centralized processor and increases the switch/network throughput. Additionally, the distributed routing decisions are based on local information, whereas the centralized routing decision are made on global and perhaps obsolete information. A hybrid of centralized and distributed routing control may provide optimal performance by combining advantages of both the techniques.

2.2.1.4 Contention Resolution and Switching

In a packet switched network, each packet has to pass through a number of nodes (switches) to reach its destination. When the packets are being switched, contention occurs whenever two or more packets are trying to leave the switch from the same output port at the same time. The contention is resolved using various techniques: deflection routing, optical buffering and wavelength conversion. If contention cannot be resolved then one of these contending packets, chosen using a certain algorithm, is passed and others are dropped.

(a). Deflection Routing: Internal conflicts between two packets can be resolved by correctly routing one packet while deflecting the second packet to another available outgoing link. Routing decisions for deflection of packets are based on destination address and packet priorities. Deflection routing techniques require that the network topology should be multi-path or re-circulatory, so that the deflected packets can be routed to the destination following an alternate path [13]. The priority of deflected packet is increased to reduce the end-to-end latency and to avoid deflecting a packet indefinitely. The number of input links to a switching node should be equal to the number of output links. Performance of this technique decreases monotonically as the number of nodes increases [7]. This degradation can be compensated either by increasing the link speed or by reducing the probability of deflection.

(b). Optical Buffering: The storage of optical data in the fiber delay lines (FDL) is known as optical buffering. This technique is classified into two basic categories: traveling and recirculating type. A *traveling type buffer* generally consists of several FDLs whose lengths are equal to the integral multiples of a packet duration T. It also incorporates optical space switches to select from the available delay lines. The storage

time of a packet is simply determined by the delay line through which the packet is propagating. A *recirculating type buffer* consists of a single FDL forming a loop with a circulation time equal to one packet duration. The storage time of a packet in such a recirculating type buffer is determined by the number of times the packet circulates in the delay line. Both types of the buffers are able to store multiple packets with the constraints that only one packet enters and leaves the buffer at any point of time.

The recirculating type buffer is more flexible than the traveling type buffer as the packet storage time is adjustable by changing the number of recirculations. On the other hand, the storage time of a traveling type buffer is predetermined by the length of FDLs. The problem associated with recirculating type buffer is that the signal has to be amplified after a few circulations to compensate for the power loss. This results in accumulation of amplified spontaneous emission (ASE) noise from the optical amplifier, which eventually limits the maximum buffering time [57]. In addition, the gain from the optical amplifier has to be carefully controlled i.e., the product of gain and the loss in one circulation should be slightly less than unity to prevent optical signal lasing.

Optical buffers can be placed at the input or output of the optical cross connects. They can be configured in different forms (Figure 2.9): (a) Fiber delay line, (b) Programmable fiber delay line, (c) Feed-forward time slot interchanger, and (d) Active switched recirculating delay line.

(c). Wavelength Conversion: Deflection routing and Optical buffering could be regarded as deflection in general, one in the space domain and the other in the time domain respectively. Both have their advantages and disadvantages: deflection is easier to implement but cannot offer ideal network performance while buffering offers better network throughput but involves more hardware and control. When combined with

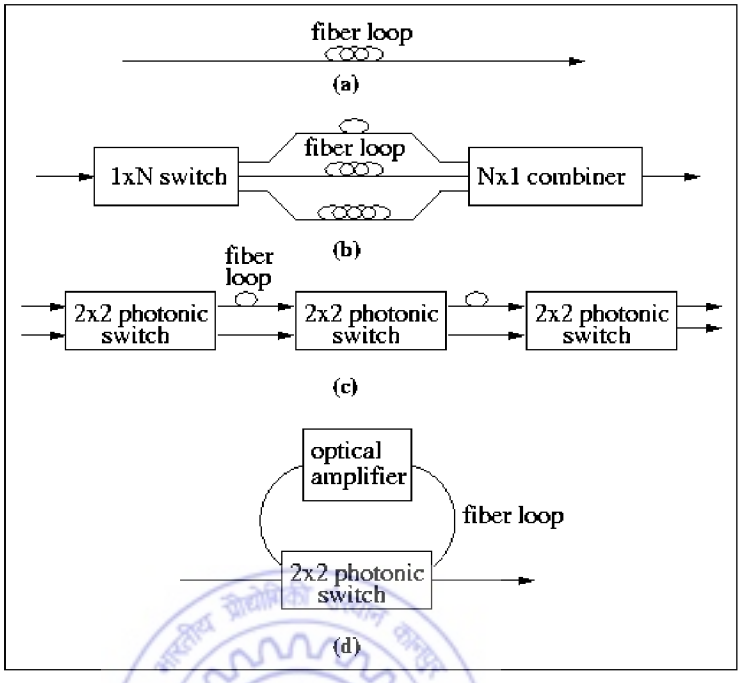


Figure 2.9: Different types of optical buffers

wavelength conversion, these disadvantages could be overcome or minimized. The wavelength domain presents one more dimension for deflection of the contending packets. In a switching node applying wavelength conversion and buffering, the input stage demultiplexes wavelength channels and the wavelength converters transfer them to available wavelength. A nonblocking space switch selects the output port or appropriate delay line for switching of these transformed packets. Wavelength conversion has been shown to reduce the number of optical buffers (Figure 2.10) and also the packet loss probability [17]. When the nodes are provided with a number of optical receivers/transmitters equal to the number of wavelengths, hot-potato routing in conjunction with wavelength conversion [8] becomes an interesting option for mesh topologies such as Manhattan Street Network (MSN) [13] and ShuffleNet [38].

However, wavelength conversion provides noise suppression and signal reshaping while the delay lines are more effective in solving contention. Therefore, the use of

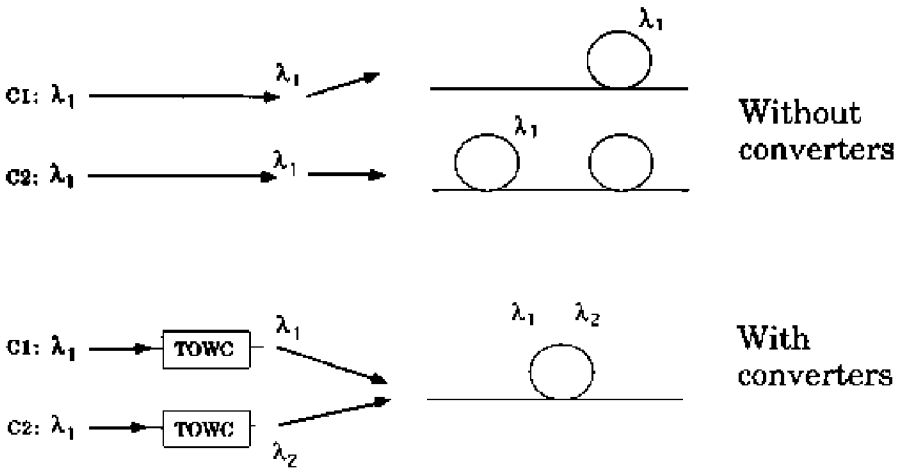


Figure 2.10: Wavelength Conversion

wavelength conversion depends on the specific network. In a network with only a small number of wavelengths, buffering might be more desirable whereas in the networks with a large number of wavelengths capacity and full wavelength conversion capabilities at nodes, buffers may not be the appropriate choice. Some times both are jointly used to utilize the advantage of optical buffering as well as wavelength conversion.

2.2.1.5 Synchronization

Synchronization is a fundamental issue that must be addressed when combining individual photonic switches into centralized or distributed switching networks [21]. In order to perform successful routing, proper alignment of packets within the switch fabric and that of headers within the RCP is needed to be done.

In general, optical packet switched networks can be divided into two categories based on synchronization: slotted (synchronous) and unslotted (asynchronous). Since the state of the switch fabric can only be changed at discrete times, it is crucial for the network designer to decide whether (or not) to have all the input packets aligned

before they enter the switch fabric. In both these cases, bit-level synchronization and fast clock recovery are required for packet header recognition and packet delineation.

In a slotted network, all the packets have same size. They are placed together with the header to form a fixed time slot. The duration of this slot will be kept longer than the total duration of packet and header. This provides sufficient guard band between packets. In most cases, optical buffering is implemented by using fiber loops or delay lines with a propagation delay either equal to or a multiple of the time slot duration. This leads to the requirement that all input packets arriving at the ports have the same size and are aligned in phase with a local clock reference. In an unslotted network, the packet may or may not have the same size. Packets arrive and enter the switch without being aligned. Here, the chance of contention is larger because the behavior of packets is more unpredictable and less regulated. Buffering in optical domain in these networks is much more complex [72]. On the other hand, these switching networks will be more robust and flexible than the slotted networks. With careful design of node architectures and protocols according to the network specifications, satisfactory performance can be achieved even in unslotted systems.

2.2.1.6 Header Regeneration

Header regeneration involves computing, generating and reinserting a header with the associated payload before it leaves the appropriate switch output port. There are several circumstances where this functionality is required e.g., in an all-optical photonic packet switch where the header is completely removed from the payload for processing, or where the routing strategies require a modification of the packet header. It is important that the header regeneration technique should be able to operate for cascaded switches and is independent of the number of switches, the packet traverses.

2.2.2 Optical Burst Switching (OBS)

Optical packet switching (OPS) technology still faces cost and technology hurdles, the most notable of which is the non-existence of random access optical buffer memory. An alternative technique named as *optical burst switching* represents a balance between circuit and packet switching [3, 11]. It provides an optical networking solution that delivers the benefits of OPS while avoiding the need of optical buffer memory and other hurdles. OBS sends control packets on separate wavelengths ahead of a variable length data burst in order to reserve the bandwidth resources as a 'burst circuit' prior to the arrival of each data burst. As the burst passes, the resources are released. Functionally, such instantaneous circuit switching avoids the need of buffer memory along the path to handle the traffic bursts. In addition, synchronization requirements are less stringent than in OPS due to looser coupling between control signals and data in OBS. Finally, since control packets are much smaller than the data payloads, one or two control wavelengths can support a large number of data wavelengths. Optical burst switching can be summarized in the following points:

a) A control header is sent first along a separate control channel to set up a connection while data packets awaiting transport are accumulated into a data burst, and are stored in electronic memory at the edge of the network.

b) After an offset time, the data burst is sent without waiting for an acknowledgment that the connection was established. This one-way reservation protocol is similar to tell-and-go (TAG) switching and results in reduced latency.

c) By choosing an offset time larger than the total processing time of the control packet all along the path, the data burst passes straight through without any

buffer requirement at any intermediate nodes on the path.

d) The ability to accumulate and send from one to thousands of packets using one control packet results in low processing and synchronization overhead per unit data.

e) In a situation when either the path is not feasible or the consumed processing time for header exceeds the offset, the burst is dropped.

The wavelength on a link used by a burst, is released as soon as the burst passes through. This allows multiple bursts to share the same wavelength on the same link in a manner that is time shared and multiplexed statistically. This yields high bandwidth utilization, high adaptivity to congestion/faults and sub-wavelength granularity for low-bandwidth customers and services. When more than one burst contend for a resource, only one burst is permitted as per the resolution algorithm.

2.3 Optical Switching Components

2.3.1 Optical Fiber

All the telecommunications were done by copper wire till 1980's i.e., before the evolution of fiber as mature technology as another form of transmission media. The optical fiber medium provides several advantages over copper e.g., lower attenuation and no electromagnetic interference. The major advantage of optical fiber is very high optical bandwidth of the order of tera-hertz (THz). Although the fibers are lighter and stronger than copper, they have some problems such as dispersion, attenuation and nonlinear refraction. A fiber consist of a core which is surrounded by the cladding, both of which

are made by pure silica glass but having different refractive index. The refractive index of the core is slightly greater than the cladding.

The transmission of light inside fiber is possible due to the phenomenon of *total internal reflection*. Alternatively, one can use Maxwell equations solutions with appropriate boundary conditions to determine the field profiles (modes) which can be guided inside the fiber. The optical fiber can be either single-mode or multimode. Modes are labelled as TE_{MN} or TM_{MN} depending upon the value of the *transverse electrical field* (E_Z) or the *transverse magnetic field* (H_Z) at the surface of the fiber core in the transverse direction. Fibers that support many modes are known as *multimode*, and those that support only one mode are known as *single mode*. The core diameter of multimode fiber is much larger than that of single mode fiber.

2.3.1.1 Optical power penalties

The propagation of light inside the fiber is affected by various types of parameters, few of these are described below.

(a) Attenuation: *Attenuation* is the decrement in the power of an optical signal during its propagation in the fiber. This decrease in signal strength is caused by absorption, scattering and radiative losses. Silica glass fibers have minimum attenuation near 1550nm (0.25dB/Km) which is the most commonly used wavelength for long haul telecommunication applications. *Radiative loss* is minimized by designing the fibers with sufficiently thick cladding ($\simeq 125\mu m$) and by minimizing bending losses. *Scattering losses* can be limited by making optical fiber using very high purity raw materials.

(b) Dispersion: Dispersion refers to the broadening of optical signals as they propagate along the fiber. As the pulses broaden, they tend to interfere with adjacent

pulses and limits the maximum achievable data rate. Also, it leads to inter-symbol interference in communication links thereby increases the BER (bit-error rate). In multimode fibers, there are two dominant types of dispersion: modal and chromatic. *Modal dispersion* refers to the fact that different modes will travel with different propagation constants and cause pulse broadening. The *chromatic dispersion* occurs because different wavelengths of light propagate at different velocities in the fiber. The single-mode fiber does not suffer from modal dispersion.

(c) Crosstalk: Crosstalk denotes any distortion of a channel caused by the presence of another channel [25, 50]. Two types of crosstalk arise in a WDM system: (i). *Heterodyne crosstalk* due to interference of small power levels that appear outside the bandwidth of the channel and cause bit error rate increment when detecting the signal of interest. It is also known as *interchannel crosstalk* where the crosstalk signal is at a wavelength sufficiently different from the desired signals's wavelength and the difference is larger than the receiver's electrical bandwidth. (ii). *Homodyne crosstalk* results from interference within the channel's bandwidth. It is also known as *intrachannel crosstalk* where the crosstalk signal is at the same wavelength as that of the desired signal or sufficiently closed to it, and the difference in wavelength is within the receiver's electrical bandwidth. Intrachannel crosstalk effects can be much more severe than interchannel crosstalk. But in both the cases, crosstalk results in power penalty.

2.3.2 Couplers

Couplers are passive optical components which are used to combine and split signals in the optical networks [50]. A 2×2 coupler consists of two input and two output ports as shown in Figure 2.11. It can be constructed by carefully fusing two fibers together

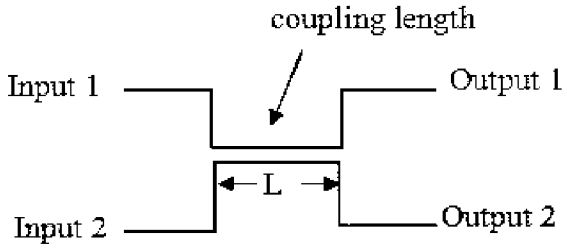


Figure 2.11: A 2×2 coupler

in the middle by keeping a certain coupling length (L). The coupler can be modelled by two parameters: a) insertion loss and b) split ratio. The coupler takes a fraction α (coupling coefficient) of the left over power after insertion loss from input 1 and places it on output 1, and the remaining fraction $1-\alpha$ is given out on output 2. Similarly, a fraction $1-\alpha$ of the left over power after insertion loss from input 2 is distributed to output 1, and the remaining power (α) to output 2. Hence, if P_1 is the power input at port 1 and P_2 at port 2 then the power output at port 1 and port 2 is given by

$$\begin{bmatrix} (P_1)_{out} \\ (P_2)_{out} \end{bmatrix} = (1-L_i) \begin{bmatrix} \alpha & (1-\alpha) \\ (1-\alpha) & \alpha \end{bmatrix} \begin{bmatrix} (P_1)_{in} \\ (P_2)_{in} \end{bmatrix} \tag{2.3.1}$$

Here, L_i is the insertion loss which happens due to scattering and coupling into radiative modes. The α depends upon the length of the coupling region.

The couplers are used to tap off a small portion of the power from the incoming signal for detecting the header of the packet and for other monitoring purposes. These are designed with values of α close to 1 i.e., 90 or 95%. The 3dB coupler is commonly known as 2×2 coupler which divides the incoming powers equally and transmits it to each of the output ports. It can be made by choosing such coupling length which provides $\alpha = 0.5$. One can also make an $N \times N$ star coupler, $1 \times N$ splitter and $N \times 1$ combiner by appropriately interconnecting a certain number of 3dB couplers.

2.3.3 Isolators and Circulators

Isolator is a device which allows transmission in one direction through it but blocks all transmission in the other direction (Figure 2.12). They are primarily used in front of optical amplifiers and lasers to prevent reflections from entering these devices, which would otherwise degrade their performance. The two key parameters of an isolator are: i) *Insertion loss* (Is) which is the loss in the forward direction and should be as small as possible and ii) *Isolation loss* (In) which is the loss in the reverse direction and should be as large as possible. The quantities (Is) and (In) can be expressed by

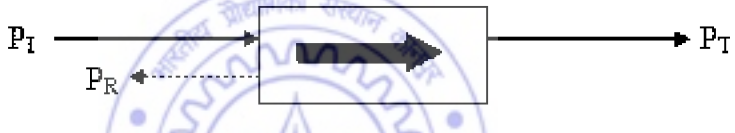


Figure 2.12: Isolator

$$Is = P_I - P_T \tag{2.3.2}$$

and

$$In = P_I - P_R \tag{2.3.3}$$

Circulator is similar to an isolator except that it has multiple ports, typically three or four. A 4-port circulator is shown in Figure 2.13. An input signal on each port is accepted by the next port and blocked by all other ports. Circulators are useful to construct optical add/drop multiplexer.

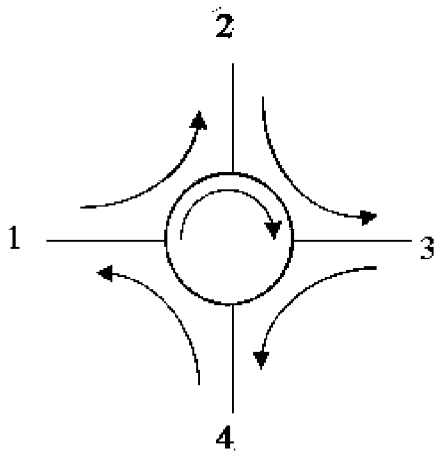


Figure 2.13: A 4-port circulator

2.3.4 Filters, Multiplexers and Demultiplexers

Filters are frequency selective components. They permit/block certain specific wavelengths and can also be used to provide equalization of amplitude distortion. For example, they are used after optical components to equalize the gain characteristic and to reduce the ASE noise. The basic purpose of filters is to reflect all but one incoming wavelengths (Figure 2.14). Multiplexers/demultiplexers are also frequency selective devices. They combine/seperate the signals using different wavelength channels.

The large transmission capacity of an optical waveguide can be utilized more efficiently by using wavelength division multiplexing (WDM) in optical communication systems. The basic concept of WDM is the simultaneous transmission of the modulated output of several light sources, operating at different wavelengths, in a single optical waveguide. Optical multiplexers consist of a multiplicity of input fibers, each carrying an optical signal at a different wavelength. All wavelengths are focused on the same focal point and are coupled into one output fiber. A WDM demultiplexer (DEMUX) separates out these signals on different wavelengths. Each signal can be

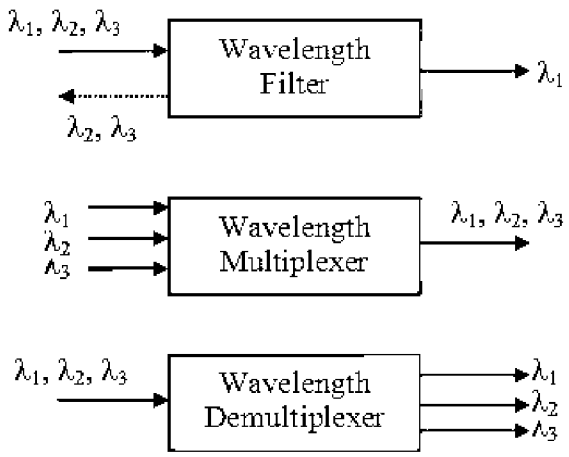


Figure 2.14: Wavelength filter, multiplexer and demultiplexer

affected by crosstalk from neighboring channels. Most optical passive demultiplexers (prism, grating, etc.) can also be used as optical multiplexers.

2.3.5 Array Waveguide Grating

An Array Waveguide Grating (AWG) is a wavelength-dependent self-routing structure. It comprises of input waveguides, an input slab, array of waveguides of different lengths, output slab, and output waveguides. The input and output slabs are star coupler (Figure 2.15). The outputs of the first star coupler are connected to the input of the second star coupler through a number of waveguides. The lengths of two neighboring waveguide differ by ΔL. The light arriving at the inputs of the first star coupler is split in equal parts. The output of the input star coupler travels in different waveguides and recombines at the output star coupler. The constructive interference of different wavelengths happens at the different output ports of the output star coupler.

An AWG of size $N \times N$ on m wavelength has a fixed routing pattern which is defined below. If the inputs of AWG are numbered from 1 to N and the wavelengths

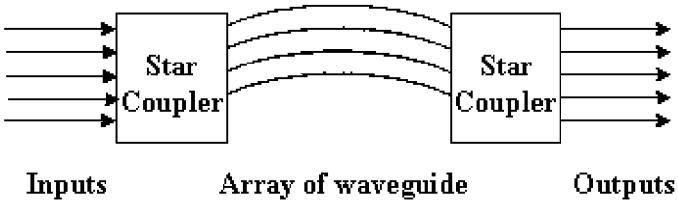


Figure 2.15: Structure of AWG

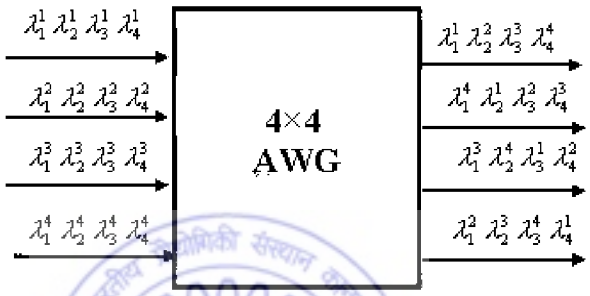


Figure 2.16: Routing Pattern of AWG

from 1 to m, then an input signal on wavelength i at input fiber j will be routed at the same wavelength on the output fiber numbered as k, where $k = [((i - j)\ mod\ N) + 1]$. The routing pattern of the 4×4 AWG, for $N = 4$ and $m = 4$, is shown in Figure 2.16.

2.3.6 Optical Cross Connect

Channel cross connecting is a key function in most communication systems. In electronic systems, digital cross-connects (DXC) are used to connect incoming digital channels to appropriate outputs. These DXCs are constructed with massively integrated electronic circuits. In all-optical networks, the information is conveyed in the optical domain through the network until it reaches its final destination. Optical cross-connects (OXC) are used in these networks as switching nodes. Optical cross-connects are devices which provide the switching of optical data in the optical domain without any O/E and E/O conversion. Generally, OXCs are constructed by using semiconductor optical amplifiers

(SOAs) [50]. The implication of SOA allows the tunability speed of the order of nano-second. Thus, these OXCs maintain data rate and protocol transparency.

2.3.7 Optical Add-Drop Multiplexer

The Optical Add-Drop Multiplexer (OADM) is another key component for dense wavelength division multiplexed (DWDM) networks. The OADM is used for selectively dropping optical signals on a specific wavelength from a transparent DWDM link (Figure 2.17) while another optical signal at the same wavelength is inserted into the empty wavelength slot. Wavelength OADM's have been proposed based on several techniques e.g., arrayed waveguide gratings (AWG) and Fabry-Perot filters. Due to the wavelength reuse scheme, crosstalk is a major problem which is associated with these devices. The crosstalk arises from coherent mixing of the signal to be received with the interfering signal components on the photo detector. This generates interference beat-noise locally at the receiver. Heterodyne crosstalk is induced due to beating between the dropped signal and the leakage from the remaining input signals at different wavelengths. The homodyne crosstalk is induced due to interference between the added signal and the leakage of dropped signal at same wavelength.

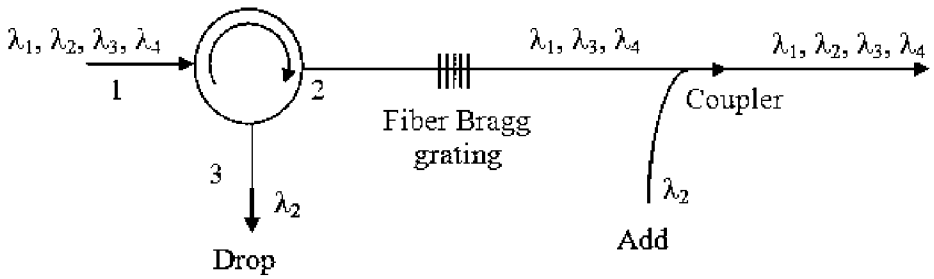


Figure 2.17: Optical add/drop element based on FBG and circulator

2.3.8 Optical Amplifier - Erbium Doped Fiber Amplifier

The incident light is amplified in the optical domain through stimulated emission using the optical amplifiers. The same mechanism was also used in lasers, but the main difference between them is that there is no feedback applied in the optical amplifiers. The optical gain depends on the frequency of the incoming signal, amount of pumping and total intensity of all the input signals. A class of optical amplifiers makes use of fiber core as a gain medium by doping it with rare earth elements (e.g., Erbium, Holmium, etc.) during the manufacturing process. Amplifier characteristic such as the operating wavelength and the gain bandwidth are determined by the dopants rather than the silica fiber which plays the role of a host medium only.

Erbium doped fiber amplifiers (EDFA) have attracted the most attention because they operate near 1550nm, the wavelength region in which the fiber loss is minimal [23]. The erbium ions may be excited by pump power at various optical frequencies e.g., 514nm, 980nm and 1480nm (Figure 2.18). These wavelengths excite erbium ions to the higher energy levels. From these levels, after staying there for approximately 1μsec, erbium ions drop to the intermediate meta stable levels, radiating phonons (the acoustical quantum equivalent of photon). Then, from this metastable level after 10 msec (spontaneous lifetime), they finally drop to the ground level emitting photons at wavelengths around 1550nm. In general, the bit rate is very high (Gbps) and the bit period is very short (nsec) compared to the long lifetime (msec) of the metastable state. Thus it does not cause inter symbol interference.

The EDFA consists of a coupler, an erbium doped fiber (EDF), two isolators and an optical pump (Figure 2.19). The optical pump is a high frequency (UV range) laser source and is used to excite rare earth ions in the EDFA. Laser light from the pump

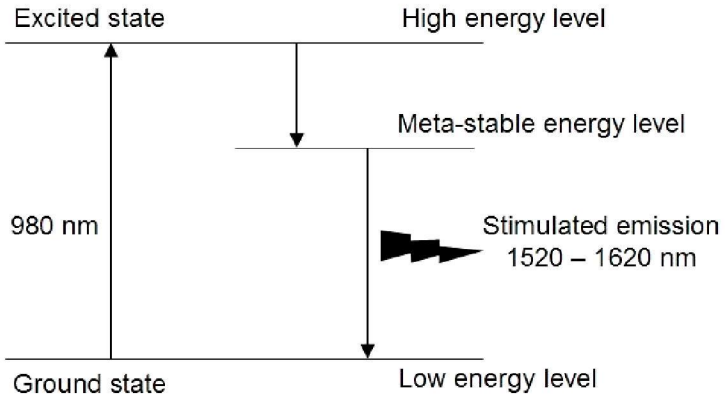


Figure 2.18: Energy level diagram for spontaneous emission of Erbium atom

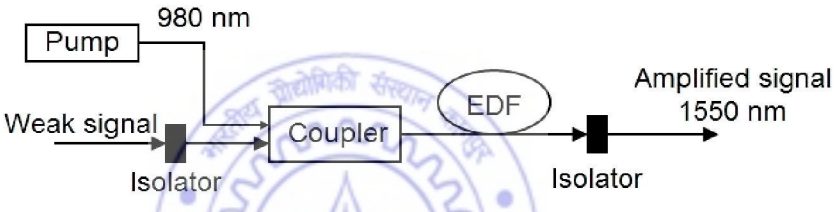


Figure 2.19: Erbium doped fiber amplifier

(980nm) is coupled into the EDF and excites the erbium atoms to higher energy level. Isolators are used to suppress the light reflections.

Advantages of EDFAs:

- EDFA can directly and simultaneously amplify a wide wavelength region (around 1550nm) with relatively flat gain (> 20 dB), which is suitable for WDM systems.
- It is commercially available in C band (1530nm to 1565nm) and L band (1560nm to 1605nm).
- It has a saturation output power level of the order of milli-Watt with a low noise figure.
- It is insensitive to light polarization and has very low sensitivity to temperature.

- It is suitable for long-haul applications.

Disadvantages of EDFAs

- The performance is affected by ASE noise.
- Crosstalk and gain saturation are also present.

2.3.9 Wavelength Converter

A wavelength converter is a device that converts the data from one incoming wavelength to another outgoing wavelength. They are very useful components in WDM networks, and can be classified based on the range of wavelengths that can be handled at their inputs/outputs ports. A *fixed-input-fixed-output* device always takes in a fixed-input wavelength and converts it to a fixed output wavelength. Other possible configurations are *variable-input-fixed-output*, *fixed-input-variable-output*, and *variable-input-variable-output*. All of them work as their name indicates.

There are three fundamental ways of achieving wavelength conversion: (i) optoelectronic (ii) optical gating and (iii) wave mixing. The latter two approaches are all-optical but not yet mature enough for commercial use. *Optoelectronic* approach is perhaps the simplest and most practical method to realize the wavelength conversion. The input optical signal is first converted to electronic form, regenerated and then retransmitted using a laser at a different wavelength. This is usually a variable-input-fixed-output converter. A variable output can be obtained by using a tunable laser.

2.4 Summary

Optical packet switching is promising because it offers much higher capacity and data transparency. Meanwhile, there has been a tremendous increase in the processing speed and the capacity of electronic switches and routers. We have discussed various basic categories of optical packet switches, where each category represents a particular switching mechanism.

The main challenges in developing photonic packet switch architectures are to achieve higher speed, higher throughput, simpler control functions, contention resolution, synchronization, etc., as well as to minimize the use of buffers. To achieve satisfactory performance of optical packet switches, significant improvements are required in developing key devices and components such as semiconductor optical amplifier (SOA), optical gates, wavelength converters, fast tunable lasers and filters, and wavelength routers. We have reviewed the various approaches and techniques for achieving photonic packet switching. It has been observed that the lack of optical equivalent of electronic memories and electronic processing capabilities has resulted in the hybrid optoelectronic implementation of photonic packet switching systems. The switching and routing fabric has generally been implemented optically, while electronic and optoelectronic components have an important role to play in functions such as address processing, switching and buffering controls.

This gives us the motivation to build an optical storage medium which can store the packet optically for the required duration. In the following chapters, we will apply different techniques of optical buffering using fiber delay lines. Our main objective is to optimize the buffer management in various switch architectures. During the initial phase, we have done few modifications in the already existing switch architectures.

Later on, we have also proposed few architectures for optical packet switching which utilize different buffering techniques.

Chapter 3

Modified Architecture for Staggering Switch

In this chapter, we propose a modification[1] to the existing architecture of the staggering switch which is an electronically controlled optical packet switch. In the proposed modification, the recirculating delay lines of one packet duration are added at the scheduling stage. The results for both the architectures (modified and unmodified) are estimated using simulations, and have been compared in terms of probability of packet loss and average delay. In the simulations, uniformly distributed random traffic has been considered.

3.1 Staggering Switch: A brief detail

The Staggering Switch [28] is an example of an "almost-all" optical packet switch where the data remains in the optical domain throughout the switch while the control operation is done electronically. The architecture of this switch is based on two stages of space switches interconnected by fiber delay lines with different amounts of delay. The

[1] "A modified architecture for the staggering switch," *Proc. NCC Conf.*, Jan' 2005, IIT Kharagpur.

delay lines act as the optical memory and are used for contention resolution. The switch follows the *output-collision-resolution* scheme based on a set of delay lines with unequal delays.

3.1.1 Switch Architecture and Operation

The architecture consists of two stages: the scheduling stage and the switching stage; both are reconfigurable and rearrangeable nonblocking switching fabrics (Figure 3.1). These stages can be implemented with electronically controlled optical switching devices (e.g., $LiNbO_3$ based coupler switch). The size of scheduling stage is $n \times m$ and that of switching stage is $m \times n$ where $m \geq n$. The scheduling stage is connected to the switching stage by m delay lines with delay d_i, where $i = 1, 2, ..., m$. The delay d_i provided by the i^{th} line equals i packet-durations. At the input of the switch, a small fraction of optical power of each signal is tapped immediately after its arrival and is passed to the detector. The detector converts it into electrical form and then forwards

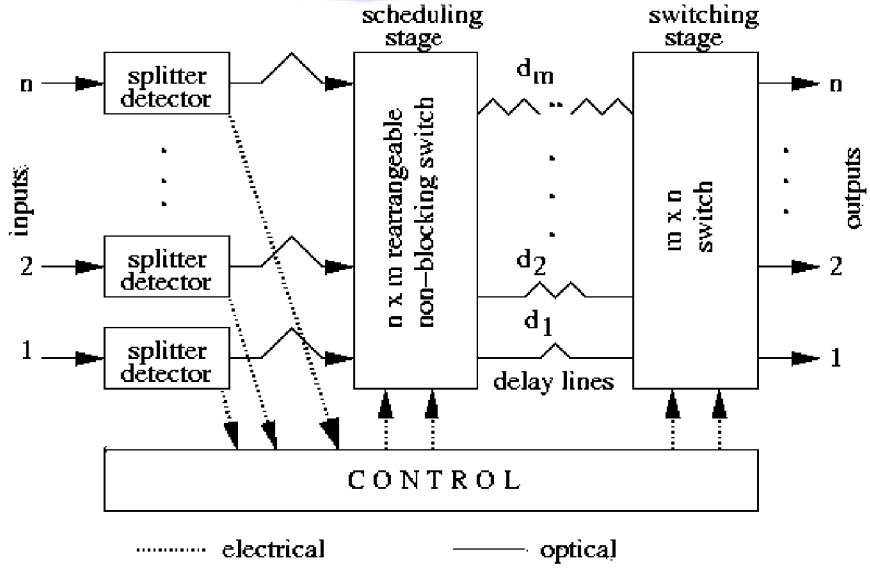


Figure 3.1: Architecture of the Staggering Switch

it towards the control section. The control section interprets the header and computes the configurations to be made in the scheduling and switching stages. The scheduling stage distributes packets to the different delay lines in such a way that no two packets destined for the same output, arrive at the switching stage in the same time slot. The delay line structure used for the scheduling of packets is shown in Figure 3.2. The input ports of the switch are scanned sequentially, and the scheduling algorithm tries to insert the packet in the lowest possible delay line subject to the following conditions:

1. no packet was inserted in this delay line beforehand in the current time slot, and
2. no other packet to the same destination exists in the column in which the packet is to be inserted.

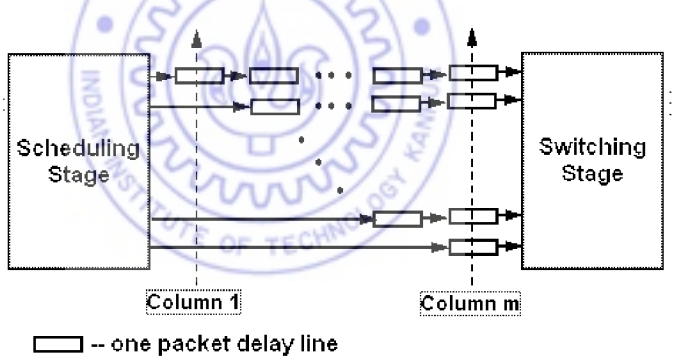


Figure 3.2: Definition of Scheduling algorithm

3.2 Description of the modification

Since the original architecture of the staggering switch does not use recirculating loops for buffering, a modification has been made to improve the performance using extra delay lines for buffering. Each extra delay line provides the delay of only one packet duration i.e., there is no recirculation. Hence, the basic principles of the switch functioning remain same and are not changed by this modification.

In the modified architecture, we are adding D extra delay lines at the scheduling stage from its output to input, thus increasing the dimension of scheduling switch to $(n + D) \times (m + D)$ (Figure 3.3). These extra delay lines will provide a delay of one packet duration which is equal to one slot [58]. These extra delay lines will store those packets which are going to be lost in the current slot due to non availability of suitable delay line d_i considering the earlier mentioned two conditions. During any time slot, a higher priority for choosing the appropriate line d_i, will be given to the packets stored in these extra delay lines. A packet stored in the extra delay lines, if it cannot be scheduled to one of the m delay lines, can again be fed to one of the extra delay lines but with a higher priority. This will avoid the indefinite delay for any stored packet. A packet will be lost permanently if it cannot be placed in any one of the m delay lines as well as in the D extra delay lines. We have estimated the packet loss probability for different values of D and compared it to the case of $D = 0$, which refers to the original architecture of the staggering switch.

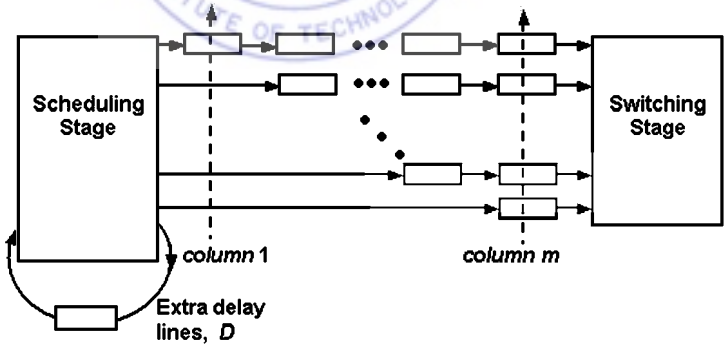


Figure 3.3: Modified Architecture

In the case of the original staggering switch, the packet loss probability decreases when we increase m beyond a fixed n. But each single increment of m, increases the delay by one slot (proportional increment of delay). This implies that the loss probability decreases at the cost of increased delay. Due to this reason, the above

modification is proposed and it is expected that this modification will reduce the packet loss probability with reasonable average delay.

3.3 Performance evaluation

The main figure of merit in the above architecture is the packet loss probability as well as the latency (average slot delay). Both depend on input line utilization (ρ), n and m, and they are affected by the variation in any of the these parameters. The performance of this architecture has been investigated for uniform random traffic as a function of ρ, n, and m. We have written the Matlab code and done the simulations to analyze the performance. Each simulation has been run for 10^6 slots to get the steady state results. These results will provide the information regarding the proper functioning of the switch.

The generation of uniform random traffic depends upon the offered load (ρ) on the system where ρ can take any value between 0 and 1 i.e., $0 \leq \rho \leq 1$. Thus the packet will arrive at the input with probability ρ and there will not be any arrival with probability $1 - \rho$. The arriving packets may choose any particular destination with equal probability i.e., for an $N \times N$ switch, each packet is equally likely to be destined to any one of the outputs with probability $1/N$.

Simulations have been done to obtain the packet loss probability and latency under various loading conditions using several combinations of delay lines. The results for the switch of size $n = 8$ are estimated for the case of $(m, D) = (8, 4)$ and (8,8), and are compared with the results for $(m, D) = (12, 0)$ to observe the effect of modifications on the actual switch of $(m, D) = (8, 0)$. The results are plotted for loss probability and

average delay versus input load for various values of m and D. The loss probability is nearly same for $(m, D) = (8, 4)$ and (12,0) while much better at $(m, D) = (8, 8)$ (Figure 3.4). The average delay is better at higher loads and remains same under lower loads for $(m, D) = (8, 4)$ and (8,8) as compared to $(m, D) = (12, 0)$ (Figure 3.5).

For the optimization of various combinations of m and D, we have computed the total buffer space available for each combination. We have also compared the size of both the stages as well as the total number of cross-points used in each case. These values are given in Table 3.1. This table indicates that the combination $(m, D) = (12, 0)$ is comparable with (8,8) but not with (8,4). The combination $(m, D) = (12, 0)$ provides larger buffer space as compared to (8,8), so the packet loss probability should be lower for (12,0). But, according to the simulation results presented in Figure 3.4, the loss probability is better for $(m, D) = (8, 8)$ as compared to (12,0). The possible reason could be unequal utilization of available buffer space i.e., the buffer space may not be properly utilized in case of $(m, D) = (12, 0)$ as compared to (8,8). Thus, we will again analyze the switch performance in the perspective of effective buffer utilization.

m	D	**Total Buffer Space** $(D + \frac{m(m+1)}{2})$	**Size of Scheduling Stage**	**Size of Switching Stage**	**Total Number of Cross Points** $((m + D)^2 + m^2)$
8	0	36	8×8	8×8	128
8	4	40	12×12	8×8	208
8	8	44	16×16	8×8	320
12	0	78	8×12	12×8	288

Table 3.1: Comparison of different parameters for various combinations of m and D at $n = 8$

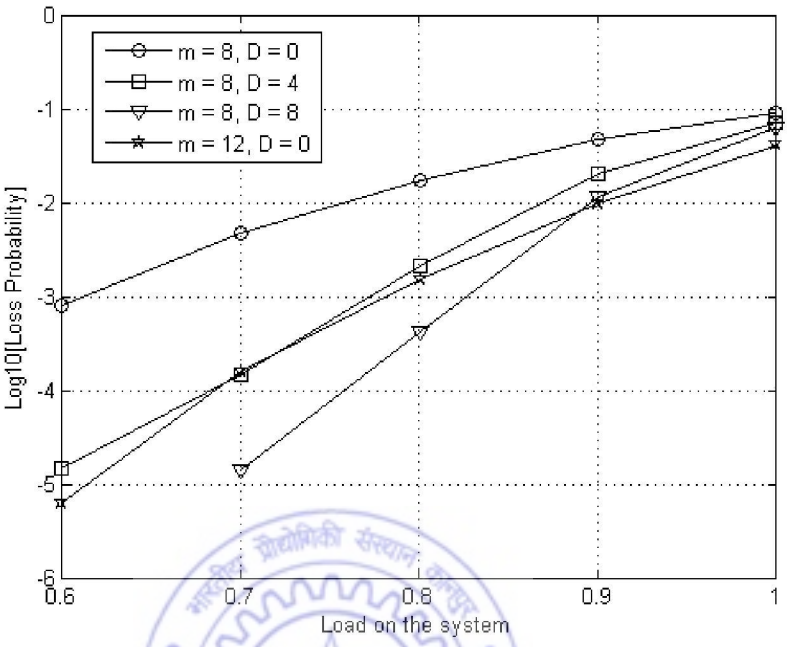


Figure 3.4: Loss probability for various values of D and m with $n = 8$

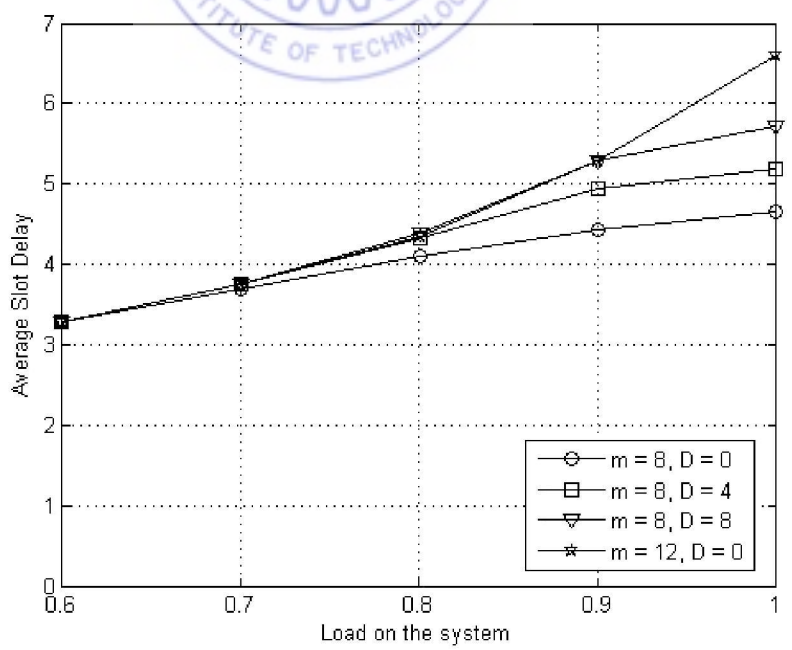


Figure 3.5: Average delay for various values of D and m with $n = 8$

3.3.1 Utilization of Delay Lines

We have again simulated the switch architecture, but this time in terms of average buffer utilization by each delay line and obtained the results as shown in Figure 3.6. We found that the buffer utilization is not very effective for longer delay lines in case of $(m, D) = (12, 0)$ as compared to (8,8) and it is evident in the plots. The theoretical value of average buffer utilization is also obtained and given in Table 3.2. This table also indicates that the average utilization of buffer space is much better for $(m, D) = (8, 8)$ as compared to (12,0). This better utilization results in the lower loss probability for $(m, D) = (8, 8)$. Hence, we can say that the adding of extra delay line will be preferable to the addition of direct delay lines.

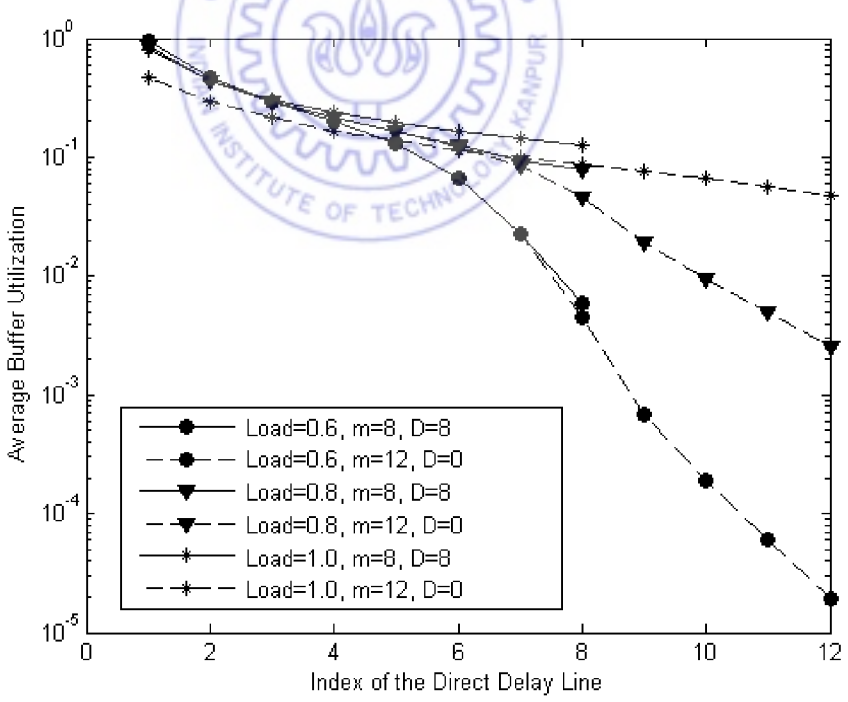


Figure 3.6: Average buffer utilization for various values of D and m with $n = 8$ under different loading conditions

m	D	$\rho = 0.6$	$\rho = 0.8$	$\rho = 1.0$
8	8	0.49	0.68	0.95
12	0	0.40	0.53	0.64

Table 3.2: Theoretical value of average utilization of delay lines for various combinations of m and D at $n = 8$

The loss probability and average delay are analyzed in terms of increasing switch sizes for various combinations of D and m. It can be observed that an increment in D (i.e., $D = n$) made better impact on the loss probability as compared to that in m (i.e., $m = n + n/2$) (Figure 3.7). Average delay variations (Figure 3.8) remain the same for an increment in D from 0 to n under all loading conditions. It follows the same pattern up to $\rho = 0.9$ for $m = n + n/2$ at $D = 0$, while there is a sudden increment in delay at $\rho = 1$ because of saturation condition.

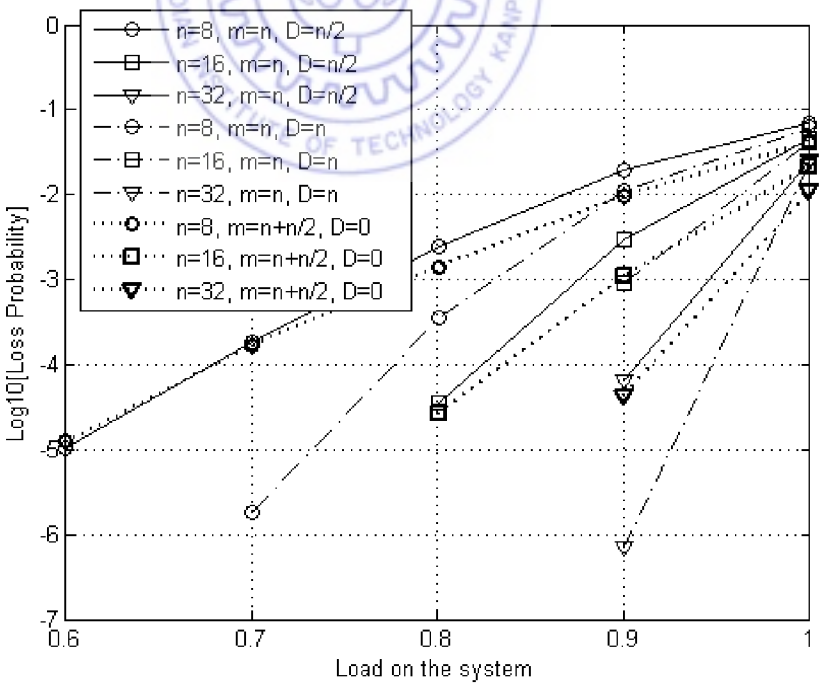


Figure 3.7: Loss probability for various D and m with increasing n

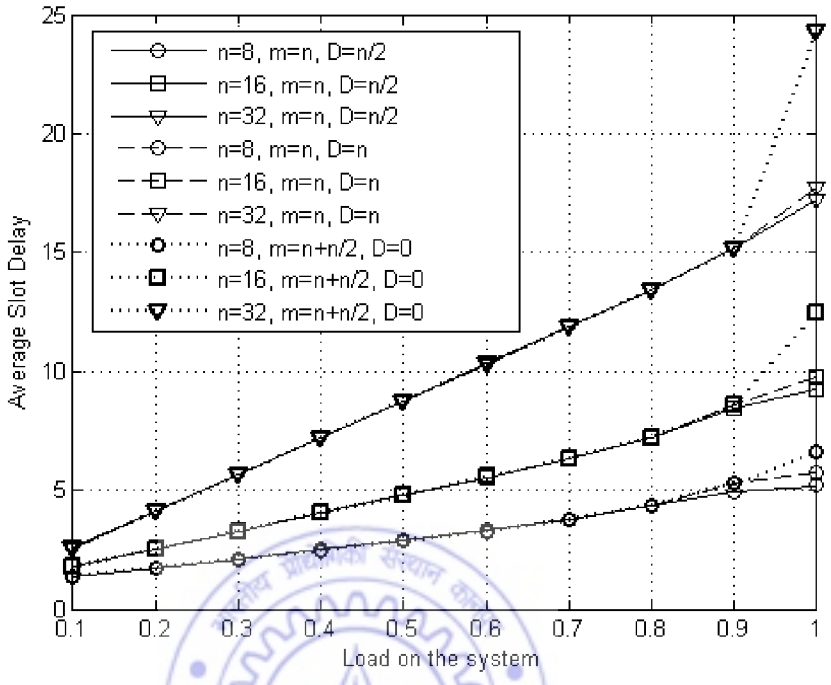


Figure 3.8: Average delay for various D and m with increasing n

From the architectural point of view, the increment in D will be more effective because any increment in direct delay lines m results in addition of a fiber delay line of that much length. For example, if value of D is to be increased from r to $r+1$ then the additional fiber will be of single delay length whereas if number of m is to be increased from r to $r+1$ then the additional fiber of $r+1$ delay length will be required.

3.4 Summary

We have discussed the proposed modification to the staggering switch. The addition of extra delay lines, has improved the switch performance. We have observed that for a fixed ρ, the loss probability is lower for larger sizes of the switch. Also, increasing the number of delay lines lowers the loss probability. The decrement in loss probability is

more for the increment in D as compared to that in m. The latency (average delay) of the switch depends on ρ. Any increment in ρ, n, and m results in an increase of the average packet delay through the switch. The delay remains relatively constant as a function of m for small values of ρ because of lower utilization, hence the extra delay lines are rarely used. However as ρ increases, the extra delay lines become more and more occupied and the average latency increases. But latency is not an issue in networks with wide span and small packet size because the propagation delay of long distance fiber may be several orders of magnitude larger than the actual switching delay.

Hence, it is advantageous to add extra delay lines instead of increasing the m beyond n to reduce the loss probability. The average buffer utilization is much better for the increment in D as compared to m. This modification will also result in the improvement of average delay performance of the whole system.

Chapter 4

A New Approach to Data Vortex Switch Architecture

The architecture of data vortex (a high capacity switch) [71] follows the principle of multiple level minimum logic network interconnect structure [51] to achieve high bandwidth and low latency. The data vortex also takes advantage of deflection routing technique [13] to resolve the packet contention. The architecture of this switch is cylindrical in shape with multiple layers. The packets will keep on rotating around these cylindrical layers whenever they cannot be directed to the desired port. In this chapter, we are proposing a modification[1] to the data vortex architecture, using fiber delay lines to improve its performance. Simulations have been done and the results are analyzed to find the advantages of proposed modification.

[1] "A new approach to the Data Vortex switch architecture," *Proc. PHOTONICS Conf.*, Dec' 2006, Hyderabad.

4.1 Data Vortex: an overview

The switch architecture (Figure 4.1 and 4.2) consists of a collection of concentric cylinders which are characterized by height parameter (H) corresponding to the number of ports located along the height of the cylinder [71]. The cylinders are also characterized by angle parameter (A) corresponding to the number of ports along its circumference at a particular height. The third parameter used in this architecture is the number of cylinders (C) which depends upon the height parameter as $C = 1 + log_2 H$. The number of ports at each cylinder is HA. At the outermost cylinder, these ports are defined as the switch input ports considering either all the ports (HA, symmetric switch) or a fraction of them (HA', asymmetric switch). Here, A' is the fraction of total number of angles (A) at each height, considered as the switch input ports whereas all the angles of this outermost cylinder are still used for routing the packets. At the innermost cylinder, the assignment of the ports as the output destinations was done by selecting only the height information, while any of the angular ports at that height can accept the packet destined for that height. All the ports on all the cylinders are still used to route the packet from the outermost cylinder towards the innermost.

During every slot, each packet moves one angle forward either along the solid line on the same cylinder or along the dotted line towards the inner cylinder (Figure 4.1). The packet moving to a port on the same cylinder will choose the height of that port by following a well defined algorithm (Figure 4.2). The packet moving to a port on the next inner cylinder will maintain the same height. But in both of these cases, the packet will be forwarded by an angle. The outermost cylinder performs a filter operation and allows the entry of only a limited number of packets through the switch input depending upon the availability of free ports. Once the packet enters the switch, it will keep on rotating

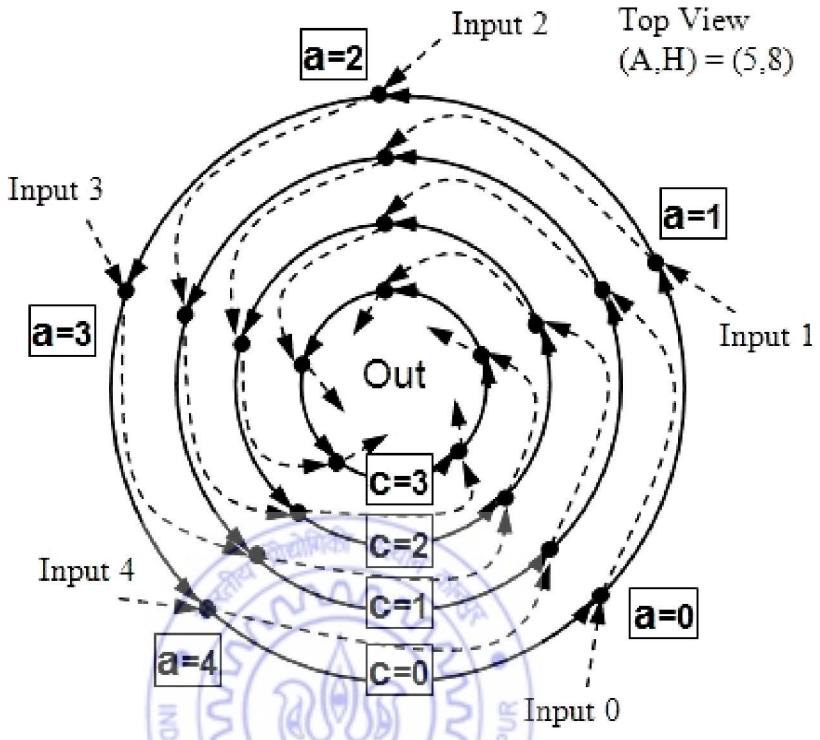


Figure 4.1: Architecture of the Data Vortex switch: *Top view* of the cylinders

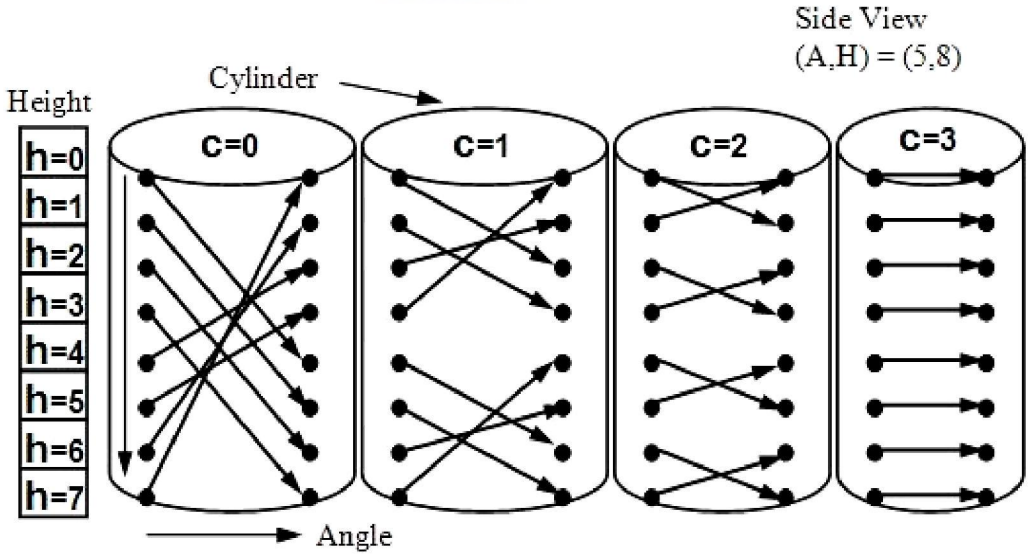


Figure 4.2: Architecture of the Data Vortex switch: *Side view* of the cylinders

at that particular cylinder until it gets space to move towards the inner cylinder. Thus there is no need of internal buffers at any of the ports. The control messages is passed to the nodes in a backward tracking manner i.e., the routing on any cylinder 'c' will depend upon the routing pattern of the next inner cylinder i.e., '$c+1$'. For example, a port P on any intermediate cylinder 'c' has two inputs (Figure 4.3), one from port Q on the same cylinder and other from port R on the outer cylinder '$c-1$'. A packet passing from port Q to P cause a control signal to be sent from port Q to R that blocks data at R going to port P. The blocked packet at port R is deflected to another port on the same cylinder. Since the control messages permit only one packet to enter a port in any given time period, it avoids the possibility of contention.

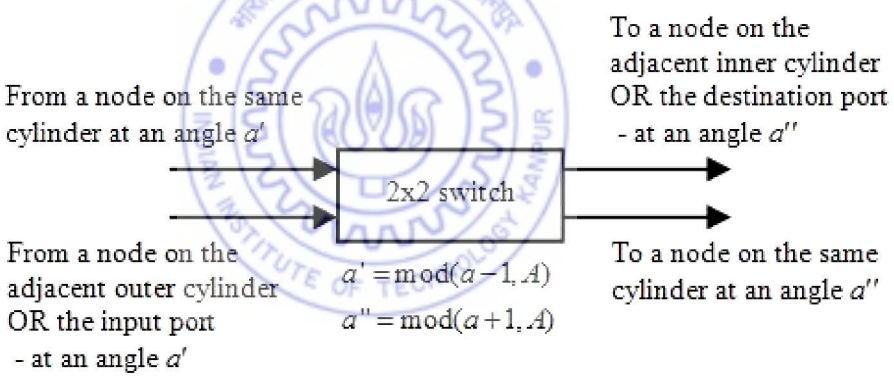


Figure 4.3: Switching port on all the cylinders

The performance of this switch can be analyzed in terms of two parameters: *Injection Ratio* (IR) and *Mean Hop Count* (Average Delay). IR is defined as the ratio of the number of successful attempts over the total number of attempts for entering into the switch at the outermost cylinder. Mean hop count is the total number of ports any packet has traveled during its transmission up to the destined output port. We have also done the analysis in terms of *Throughput* of the switch, which was not analyzed in the earlier studies.

4.2 Description of the modification

The results for the Data Vortex switch show that the injection ratio (IR) is much better under lower loading condition [71]. The IR deteriorates heavily at higher loads and this degradation in the IR is more for larger size of switches. Thus, to improve the performance of this switch, we are proposing a modification by adding extra delay lines at every input port.

4.2.1 Addition of extra delay lines at every input port

Any incoming packet may find the input port to be busy due to the specific routing nature of switch. In such a case, the incoming packet will be dropped, which results in lowering the IR. Thus fiber delay lines (FDL) have been added to store the packets [31] which will otherwise be lost due to the busy input port. These extra delay lines are added to each input port at the outermost cylinder (Figure 4.4 and 4.5) [61]. The length of these delay lines (D) is equal to one packet length which is equal to a single time slot duration. The value of 'D' represents the number of such delay lines. Since the traffic is probabilistic in nature, there may be a few slots when there will be no arrival at some of the input ports. Those input ports utilize these free slots to forward the packets stored in their corresponding delay lines. While checking for the incoming packets during every slot, the controller firstly scans the extra delay line for stored packet and then the input port for newly arriving packet. If there is any packet already stored in the FDL then that port will consider it first for routing. The new incoming packets will be forwarded to the vacant delay lines, and will be routed in the next slot. This will avoid any indefinite delay for the packets stored in these delay lines. Also, any packet at the input port with a higher priority will be routed first irrespective of

the packet stored in FDL. If an incoming packet finds the input port busy as well as the corresponding FDL is filled completely, then it will be dropped and considered as a lost packet.

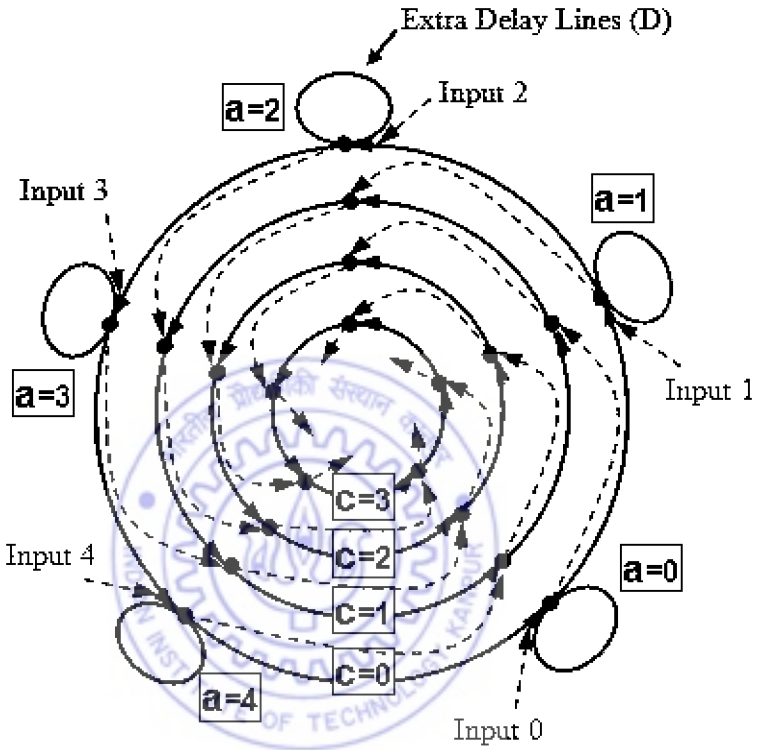


Figure 4.4: Modified Data Vortex switch (Top view)

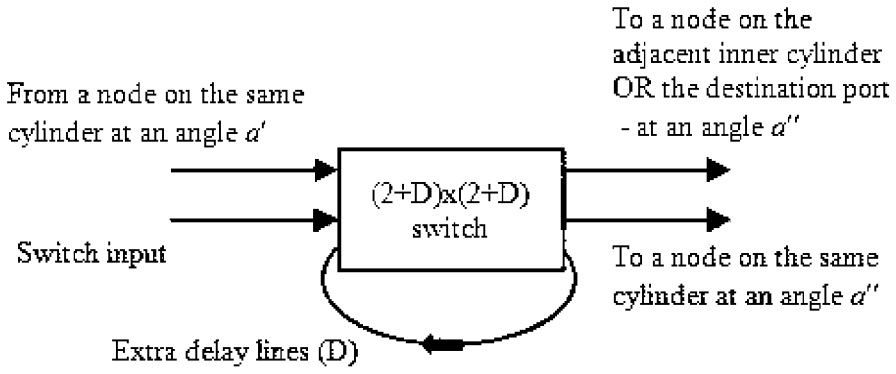


Figure 4.5: Modified switching port on the outermost cylinder. Other switching ports will remain same as shown in Figure 4.3

4.2.1.1 Performance evaluation

The simulation results for injection ratio (IR) and mean hop count (average delay) under different loading conditions are shown in Figure 4.6 and 4.7 respectively. We also compare these parameters for various heights of cylinder. Here, $D = 0$ shows the case of data vortex without modification. When we add a single delay line ($D = 1$) at each input port, the improvement in IR is better, but only under low and moderate loading conditions (Figure 4.6). The IR improvement is more for cylinders of shorter heights as compared to the larger heights. The average delay is more for larger cylindrical heights under moderate loading (Figure 4.7).

The switch has also been analyzed using the height parameter and it can be noted that the advantage due to addition of extra delay lines disappears when H is large (Figure 4.8). The effect on switch performance with asymmetric data is also shown in the same figure. This time, the addition of extra delay lines leads to better IR even for higher heights. The addition of extra delay lines has a slight effect on the mean hop count for symmetric and asymmetric data under moderate loading conditions (Figure 4.9). Thus we can say that this modification will work properly for cylinders of heights up to $H = 128$ and under moderate loading conditions. Still, under lower loading conditions (i.e., $\rho < 0.6$) and for asymmetric data, cylinders with larger heights take advantage of these extra delay lines.

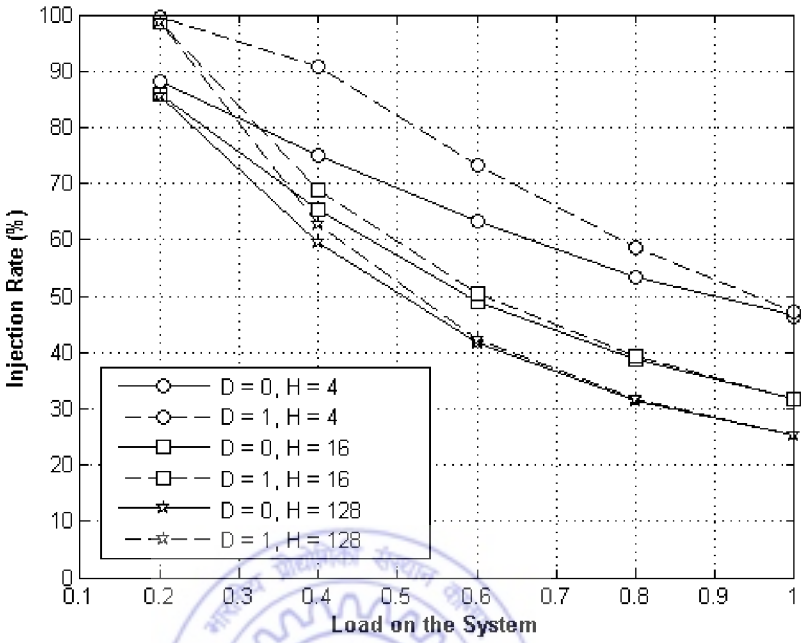


Figure 4.6: Injection Ratio after adding a single extra delay line for $A = 5$. *Straight line*: Actual results, *Dashed line*: Modified results

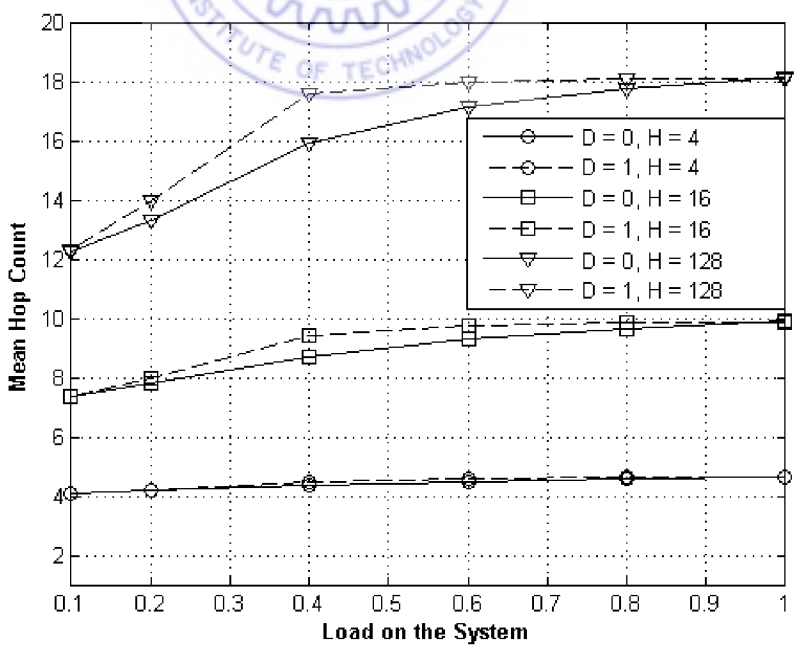


Figure 4.7: Average Delay after adding a single extra delay line for $A = 5$. *Straight line*: Actual results, *Dashed line*: Modified results

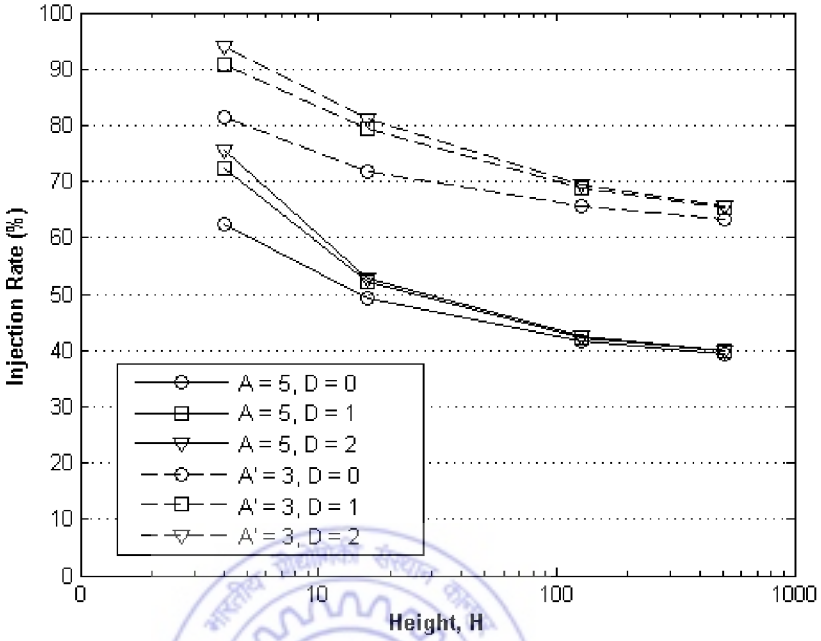


Figure 4.8: Modified results for IR with Height under $\rho = 0.6$. *Straight line*: Symmetrical data, *Dashed line*: Asymmetrical data

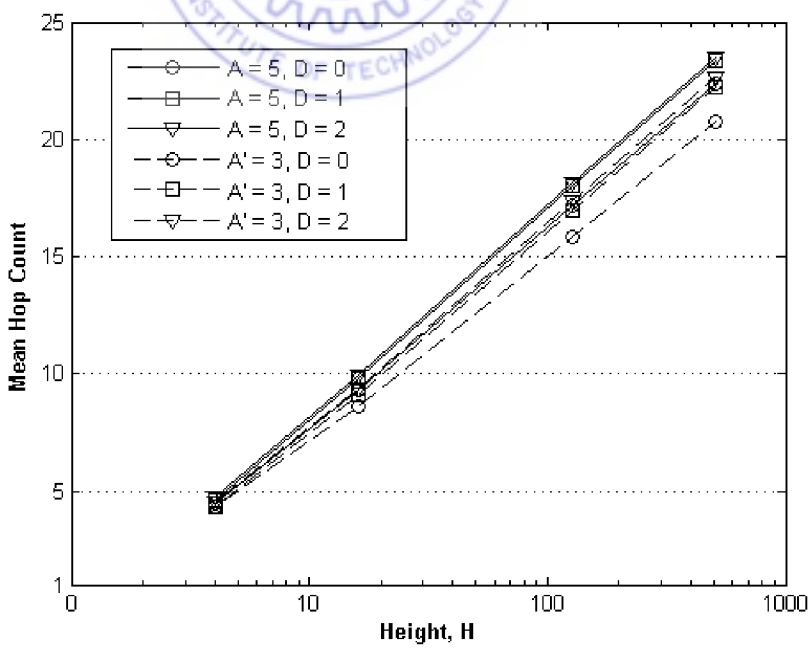


Figure 4.9: Modified results for Average Delay with Height under $\rho = 0.6$. *Straight line*: Symmetrical data, *Dashed line*: Asymmetrical data

4.3 Throughput Analysis

We have analyzed the performance of the original switch as well as the modified one, in terms of *Throughput*. This study was not done in the original literature. We observe that there is a maximum limit on the throughput, achieved for all the heights (Figure 4.10 to 4.12). The system throughput is always smaller than the real load.

The throughput becomes constant after a certain load for larger heights of the cylinders (Figure 4.10). We found that the maximum throughput for $H = 4$ is 47% at $\rho = 1$. The value of this maximum attained throughput decreases for larger heights.

In case of the modified architecture, the throughput rises for various values of D, but only under the moderate loading conditions (i.e., $0.3 \leq \rho \leq 0.7$) while it will remain same for much higher ($\rho \geq 0.8$) and much lower loads ($\rho \leq 0.2$) (Figure 4.11). The reason is that:

1. at lower loads, since very less number of packets are arriving and they will be easily accommodated by the already available space in the switch, while
2. at higher loads, the saturation will be achieved due to which there will not be any effect of adding extra delay lines.

We have also observed that for $H = 16$ and $\rho = 0.3$, the throughput increases significantly up to $D = 4$ while it become constant for $D \geq 5$ (Figure 4.12). Hence, there is not much advantage of adding extra delay lines beyond a certain number.

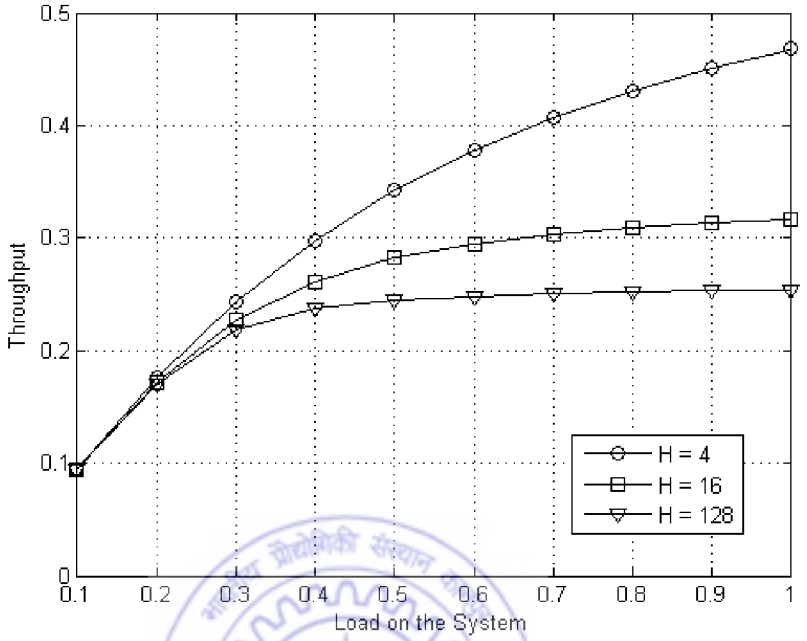


Figure 4.10: System 'Throughput' under symmetrical data for $A = 5$.

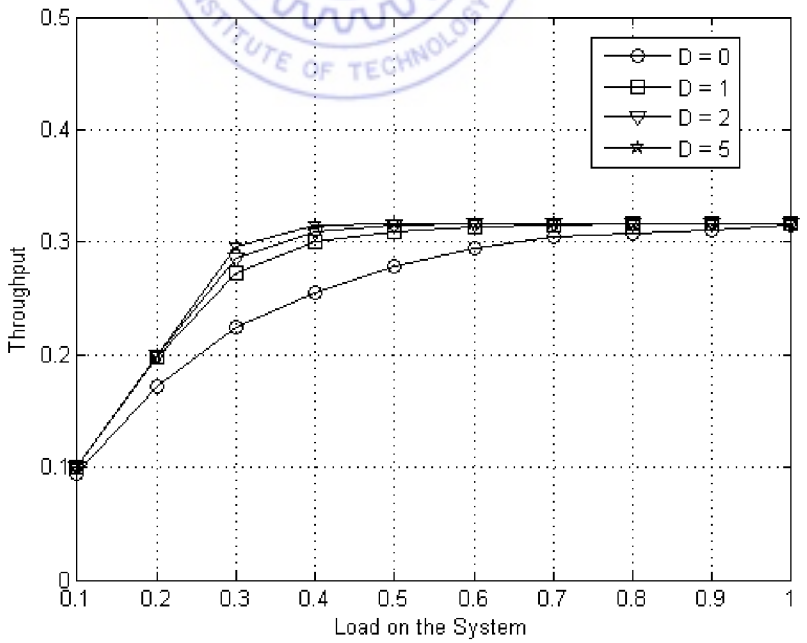


Figure 4.11: Modified results for system 'Throughput' for $A = 5$ *and* $H = 16$ for various values of D.

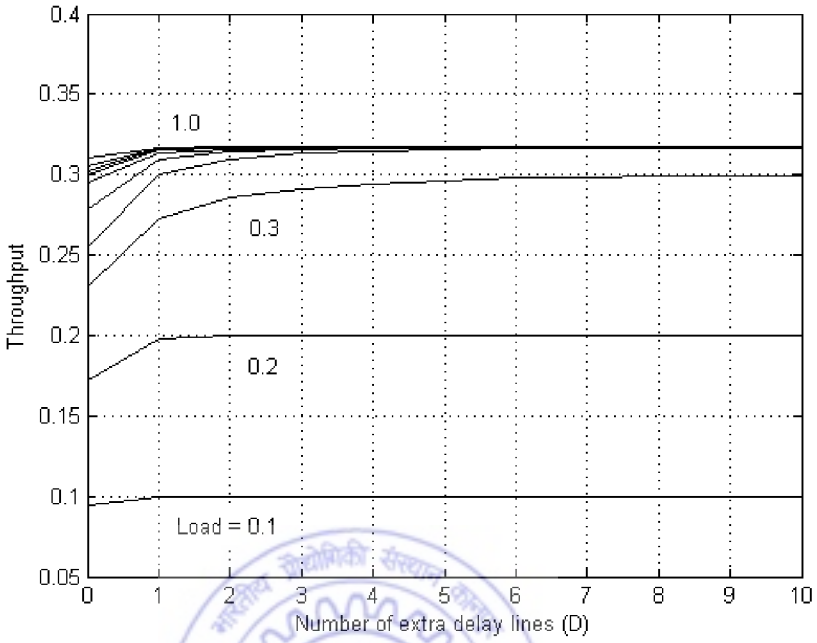


Figure 4.12: Modified results for system 'Throughput' for $A = 5$ *and* $H = 16$ at various loads.

4.4 Summary

In this chapter, we have proposed a modification to the existing architecture of the Data Vortex switch, by adding extra delay lines at each input port. The actual and modified switch have also been analyzed in terms of system throughput.

The simulation results indicate that modification proposed to the Data Vortex switch is feasible and the switch is scalable under such conditions. The cost of a few fiber delay lines, whose length is equal to the packet length, will not be too high. Also, this cost will be overshadowed by the advantages we are getting in terms of better injection ratio (IR), reasonable average delay and increased throughput.

Chapter 5

An Architecture for Optical Packet Switch based on WDM Loop Buffer Memory in feedback configuration

In this chapter, we propose an optical packet switch architecture[1] which uses loop buffer modules [55, 66] in feedback configuration. WDM based fiber delay lines are used to store the contending packets and a space switch fabric is used to direct them appropriately. These delay lines incorporate various optical components which induce power loss in the signal during its revolution in the loop.

Our objective is to analyze the switch performance in terms of the packet loss probability and average delay, so as to verify the proper functioning of the proposed switch. We have done the power budget analysis, taking care of various types of noise in the loop buffer module, to calculate the number of maximum allowed circulations for a packet in the loop buffer before its correct reception. The simulation results for packet loss probability and average delay are obtained by using a specific scheduling algorithm. The mathematical analysis is also done to validate the simulation results.

[1] "Wavelength Division Multiplexed Loop Buffer Memory based Optical Packet Switch," *Opt. Quant. Electron.*, Vol. 39, No. 1, pp. 15-34, 2007.

5.1 Description of the switch

The proposed optical packet switch architecture [62] is shown in Figure 5.1. The core of this architecture is a nonblocking space switch of dimension $2N \times 2N$ (Figure 5.2). The lower N ports (indexed 1 to N) of the core switch are used as switch inputs/outputs and the upper N ports (indexed $N+1$ to $2N$) are used for buffering of packets in the optical loop buffer modules. In this configuration, the maximum number of allowed buffer modules is $m = \lfloor N/D \rfloor$, where D is the number of inputs/outputs for each loop buffer module. Thus D and hence m will depend upon desired packet loss probability.

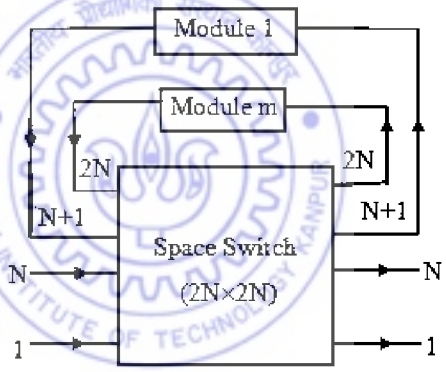


Figure 5.1: Optical packet switch architecture. Modules (1 to m) represent optical loop buffer memories.

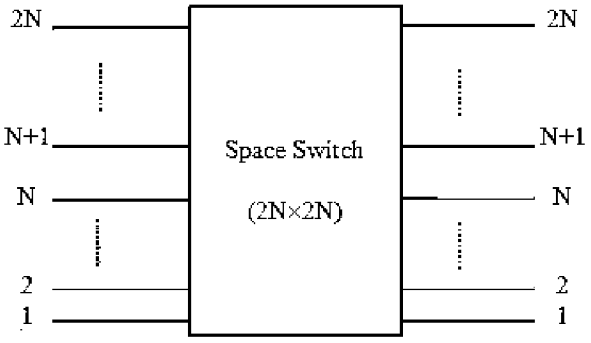


Figure 5.2: Architecture of the core switch.

If the switch is designed for M modules ($M \leq m$), then the rest of the upper half ports (i.e., $N - MD$) will be left free. Hence, the effective size of the core switch will become $(N + MD) \times (N + MD)$. In the performance analysis of the switch, we have assumed the length of the delay line as well as the slot duration to be equal to one packet length. Newly arriving packets and already stored packets may contend for the same output. In such a case, one of the contending packets is directed to the output port and the remaining packets are kept in buffer according to the scheduling algorithm given in the following section. When the contending packets can neither be directed to the assigned output port nor stored in the buffer, they are dropped and assumed to be lost.

Each buffer module (Figure 5.3) consists of D Tunable Wavelength Converters (TWC) at its input, one $D \times 1$ Combiner, one recirculating loop, one $1 \times D$ Splitter and D Fixed Filters (FF) at its output [55, 66]. The path followed by a packet, during one circulation in the recirculating loop, consists of a 3dB coupler, $1 \times B$ DEMUX, TWC, $B \times 1$ Combiner, EDFA, Isolator and again the same 3dB coupler. The number of TWCs and the size of DEMUX/Combiner inside the loop will be equal to the required

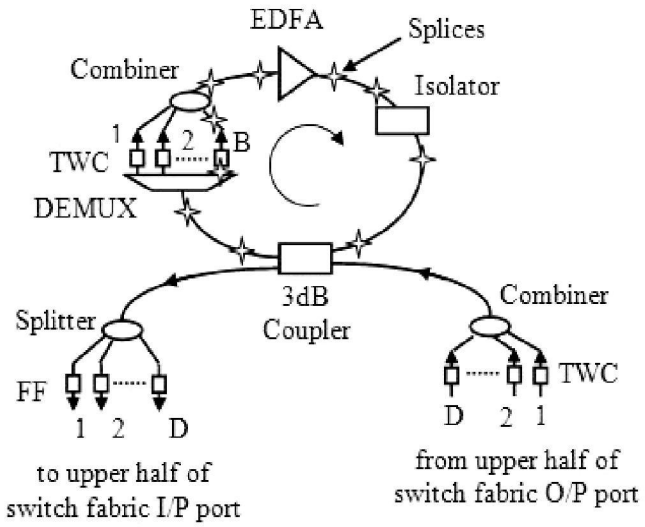


Figure 5.3: Loop Buffer Module.

buffer capacity. Thus the total number of TWCs and FF used in the buffer module will be $(B + D)$ and D respectively. An EDFA is placed inside the recirculating loop of each buffer module to compensate the signal power loss during circulations in the loop buffer.

5.2 Working of the switch architecture

Each buffer module uses $(B + D)$ wavelengths where B is the number of buffer wavelengths used to store a packet in the buffer, and D is the number of wavelengths used for reading out the packets from the loop buffer. The packets passing through the inputs of buffer module use WDM technology to share the recirculating loop buffer. The number of buffer wavelengths inside the memory module is decided by the switch design, desired traffic throughput, packet loss probability and size of the switch [73]. The allocation of packets to the loop buffer depends on the routing and priority algorithm for the switch. The packets to be stored in the loop buffer are converted to the wavelengths available in the buffer modules; if the buffer is full then the packets are dropped. When a packet is forwarded for buffering, the respective TWC at the input of the available buffer module is tuned to any one of the available loop buffer wavelengths (B). As long as a packet remains in the buffer, the TWC inside that module corresponding to the wavelength assigned to this packet, will remain transparent. For reading out a packet when the output contention is resolved, the corresponding TWC is tuned to the wavelength of appropriate output port fixed filters (FF), and then the packet is broadcasted towards them. The FF at the intended output will allow the packet to pass through, and other FFs will discard it. Then, these packets will be directed to the destined output port through the space switch fabric.

We have assumed an electronic control unit (not shown in the figure) which tunes various components in the loop buffer as well as controls the whole switch. A similar type of electronic control technique has been described in [15]. The control of packet buffering can be done by this controller according to the scheduling algorithm given in following section. We have considered SOA based TWCs which are proposed and fabricated in [15]. These TWCs are operated on the *nano-second* scale. The space switches are considered as SOA based electro-optical switch. The switching speed of this device is also of the order of *nano-seconds* while the insertion loss will be 0.5dB per stage. The crosstalk will be low (-30dB) and hence, neglected in the calculation [44]. Thus, the tuning speed of TWCs and the switching speed of space switch do not put any constraint on the switching operation.

How the buffer wavelengths are cleared from the loop buffer:

This paragraph explains the clearance of used buffer wavelength, once the buffered packet is delivered to the intended output port. While sending the packet into the loop through the 3dB coupler, half power of the packet is transmitted to the loop (Figure 5.3) and another half of the power is passed directly to the FFs. But, these FFs are chosen to receive the wavelengths of range D, so it will discard the wavelength coming directly from loop buffer input (not from the loop), because the range of these wavelength corresponds to B. Similarly, while reading out the packet from the loop, the TWCs inside the loop tune the packet to any of the D wavelengths, which then passes through the 3dB coupler. Half of the power of this packet will be passed towards the FFs, and remaining half power will again enter the loop. But, this half power entering the loop is discarded by the DEMUX present inside the loop because the wavelength range of this DEMUX is B. At this point, the buffer wavelength gets freed-up for storing a new packet. One should note that the read/write operations can be done simultaneously.

The optical components placed inside the recirculating loop of the buffer module will affect the signal quality by adding various types of noises during each revolution. Thus, more the circulations performed by the signal, more is the noise and so is the degrading factor affecting the signal quality. If the losses through these components are considered, it will limit the number of circulations. In the earlier investigations, the effect of maximum circulation limit has not been taken into account. It will be desirable to analyze the switch performance considering the recirculating limits. For the sake of clarity, we will first discuss the switch behavior without any circulation limits. Later on, the effect of circulation limit will be considered and discussed.

5.3 Switch without circulation limit

After the conceptualization of this proposed switch architecture, we found an architecture in [6] which is worth mentioning here. It also uses space switch and fiber delay lines, but the use of loop buffer modules makes our architecture different. The major differences and advantages are as follows:

- *Better routing strategy*: Each stored packet is passed through core switch fabric for multiple times during its re-storage in case of [6]. While in the architecture proposed here, the stored packets are passed through the core switch only once i.e., when it has to be routed to the intended output.

- *Wavelength reuse*: We are using several modules of fixed capacity and all these modules are placed independent of one another i.e., they do not communicate among themselves. Hence, we can use the same set of wavelengths in each module. Thus, the maximum number of required wavelengths will be equal to N/M ($\simeq B$)

whereas if the switch shown in [6] will use WDM then the maximum number of required wavelengths will be equal to the number of used delay lines i.e., N.

5.3.1 Scheduling algorithm

Firstly, we will define two ***constraints*** depending upon the buffer capacity. These are:

1. The number of buffered packets (x_j) for the output j should never be greater than the maximum buffering capacity ($= M \times B$) i.e., $x_j \leq MB$ for $1 \leq j \leq N$.
2. Total amount of buffered packets (adding for all the outputs) cannot be larger than the maximum buffering capacity i.e., $\sum x_j \leq MB$.

The buffering in the modules, is done using the following scheduling algorithm:

1. The TWCs placed at the inputs of loop buffer can be tuned to any of the B wavelengths. The TWCs placed inside the loop can be tuned to any of the $(B+D)$ wavelengths. It is assumed that TWCs can be tuned almost instantaneously.
2. If there are total i packets buffered in all the modules for the output j, then one of them will be sent to the output through the switch fabric. If in that slot, one or more packets are also present at any of the inputs of switch, destined for the same output j, then they will be buffered in the loop buffer to the extent allowed by constraints 1 and 2.
3. Considering the case when there is no packet in the buffer for the output j, but n of N input lines have packets for this output. Then, one of these n packets is directly sent to output j and the remaining $(n-1)$ packets will be stored in the buffer module to the extent allowed by constraints 1 and 2.

4. The buffer management allows simultaneous read/write in the same time slot for common wavelengths in any of the buffer module.

5. The contending packets will try to occupy the lowest numbered (1 to m) available buffer module.

6. During any time slot, priority will be given to the packets stored in the loop buffer modules over the packets arriving at the switch input.

7. If there are total q packets in all the modules for any output r, then the oldest of q contending packets, will leave first for the switch output. Essentially, the FIFO discipline will be maintained.

8. Packets for different output can leave the modules at the same time.

9. If any of the incoming packets is not be able to pass through the switch due to the maximum buffer capacity limitation, then it will be dropped.

10. The contending packets will be stored in the buffer module subject to the constraints specified in the constraints 1 and 2. There can be many strategies for storing the packets. Simplest is to find the lowest numbered module which is empty, and store the packet in it according to the constraints 1 and 2. We have considered this algorithm in this work. Another alternative approach could be to find out the module with minimum number of packets and store the packet on a wavelength such that wavelength spacing for stored packet in the loop buffer is maximized. This larger available spacing between wavelength used for storing packet will imply less crosstalk due to imperfect filtering characteristics of various devices.

This scheduling algorithm can also be understood by the flow chart as shown in Figure 5.4.

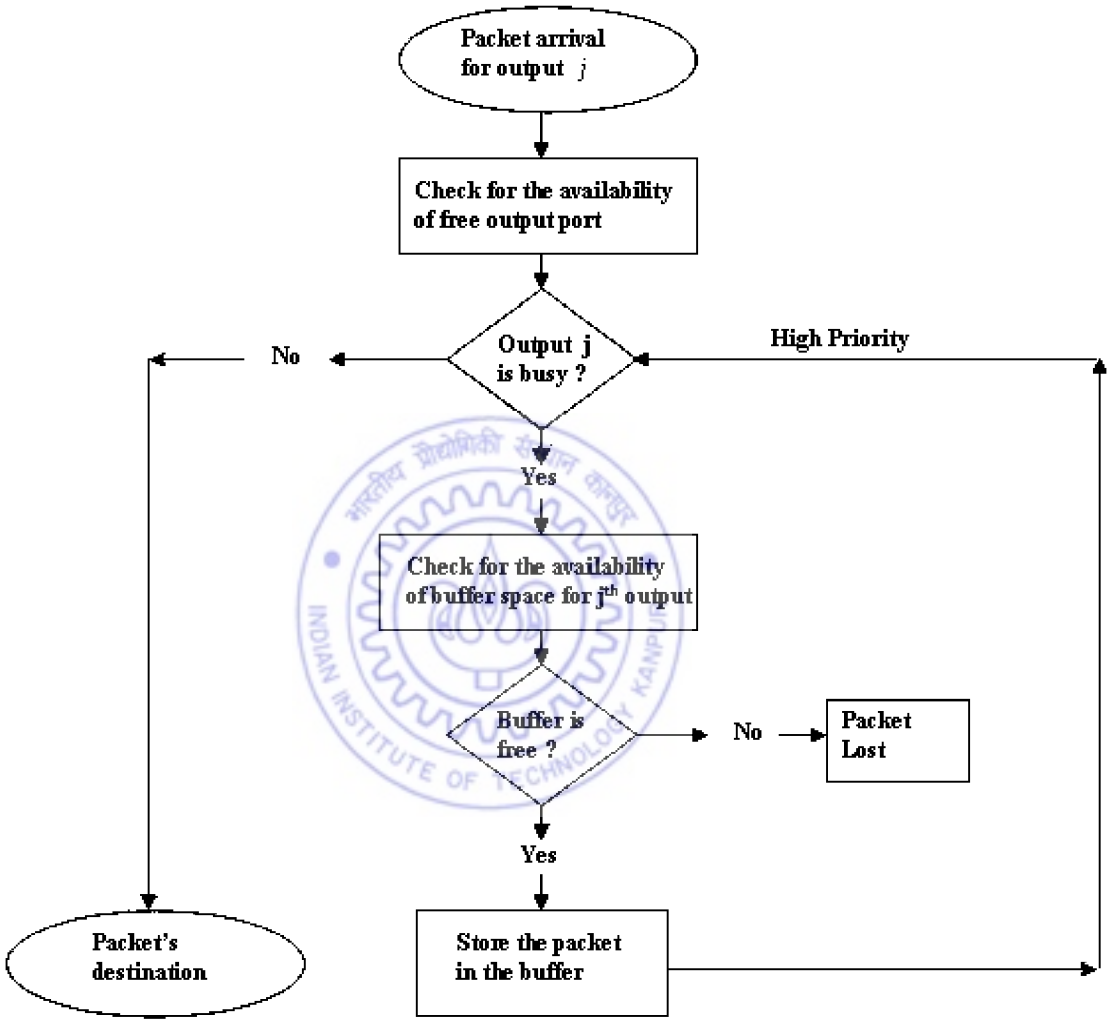


Figure 5.4: Flow Chart for the Scheduling Algorithm

5.3.2 Performance Analysis and Results

Using the above algorithm, the simulated results for '*packet loss probability*' and '*average packet delay*' were obtained under various loading conditions to determine the effect of

using different number of buffer modules (M). The results for the switches of various sizes are shown in Figure 5.5 to 5.8. As defined earlier, the size of switch fabric is $2N \times 2N$ where lower N ports are the actual inputs/outputs and upper N ports are used to connect different number of buffer modules.

We can observe from Figure 5.5 that under lower loading conditions, the packet loss probability decreases with increase in N. While for higher loads, the packet loss probability is almost same for all values of N. The number of buffer module is maximum (i.e., $M = N/D$) for each size of switch, and the buffering capacity (B) is same for each buffer module of all the switches. One can further observe that the ratio of total number of buffers to total number of inputs remains same (i.e., $MB/N = 1$) for each switch because $B = D$. Since it is decided that all the buffer modules are fully shared, so the number of buffers required per input port reduces with the increase in switch size. The reason behind this reduction is the probability of K packets, destined for a particular output, out of N arriving packets will reduce with an increase in N. The proof of this statement is as follows.

During any slot, a maximum of N packets can arrive and that will happen at maximum load (i.e., $\rho = 1$). Now, let us consider $P(k)$ as the probability that k out of N arriving packets, are destined to the same output. It can be expressed as

$$P(k) = {}^{N}C_{k} \left(\frac{\rho}{N}\right)^{k} \left(1 - \frac{\rho}{N}\right)^{N-k} \tag{5.3.1}$$

This probability will be decreased by the increment in the value of k for a particular ρ. In the worst case of $k = N$, the probability $P(k)$ will become

$$P(N) = \left(\frac{\rho}{N}\right)^{N} \tag{5.3.2}$$

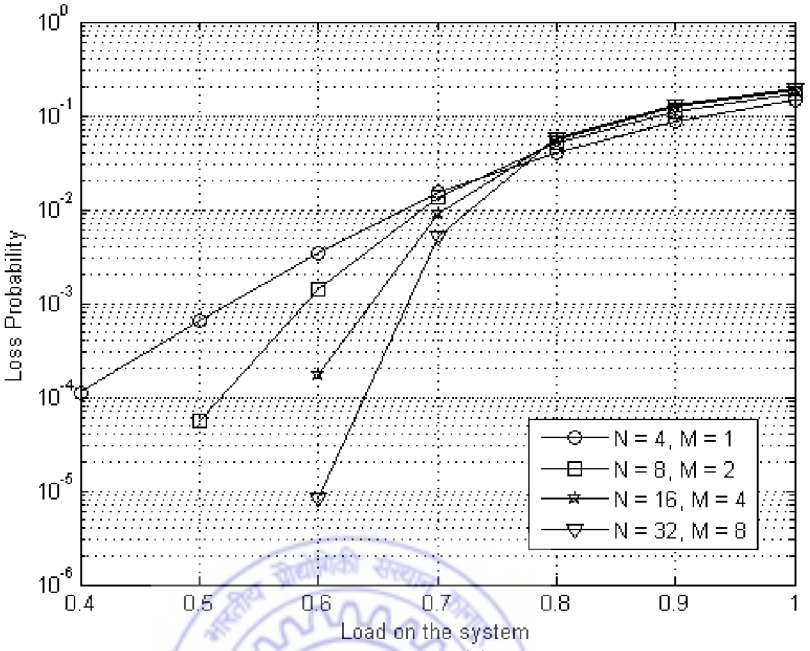


Figure 5.5: Number of module is maximum for each case at $B = 4$.

For higher values of N, we can write

$$P(N+1) = \left(\frac{\rho}{N+1}\right)^{N+1} \tag{5.3.3}$$

If we compare the effect of increase in N, on the probability term, then

$$\frac{P(N+1)}{P(N)} = \frac{(\rho/(N+1))^{N+1}}{(\rho/N)^N} \tag{5.3.4}$$

$$= \frac{\rho}{N}\left(\frac{N}{N+1}\right)^{N+1} \tag{5.3.5}$$

For larger values of N, $(N+1) \approx N$, thus

$$\frac{P(N+1)}{P(N)} = \frac{\rho}{N} < 1 \tag{5.3.6}$$

Hence, $P(N+1) < P(N)$ and we can say that the probability will be decreased for

every increment in the value of N. This results in lower requirement of buffer, and finally the loss probability will become smaller with larger values of N.

Figure 5.6 shows the effect of increasing the number of buffer modules, as the fraction of its maximum value, on the loss probability. All the results show that the loss probability decreases with the increment in either the number of modules or the switch size. This indicates that the buffer requirement per port reduces with increasing switch size under moderate loading conditions. This result is expected because of the above mathematical proof.

Average delay performance for various sizes of switch under different loading conditions is shown in Figure 5.7. The delay remains nearly same for all the switch sizes under moderate loading. Also, there is not much difference in the value of average delay for higher loads. The average delay performance with different number of modules in the architecture is shown in Figure 5.8. We observe that on increasing the number of modules, the average delay increment is very low and becomes nearly constant after a certain number of modules. The larger switches have more packets at the input as compared to the smaller switches, at all loads but at the same time, they also have more space to accommodate the packets. So, the delay variation remains nearly same for all values of N.

For the verification of the simulation results, the curves have been plotted in the Figure 5.9 which shows the probability of packet loss at different values of M for the switch of size $N = 8$. This simulation result follows the results for $N = 8$ obtained by the mathematical model presented in [6].

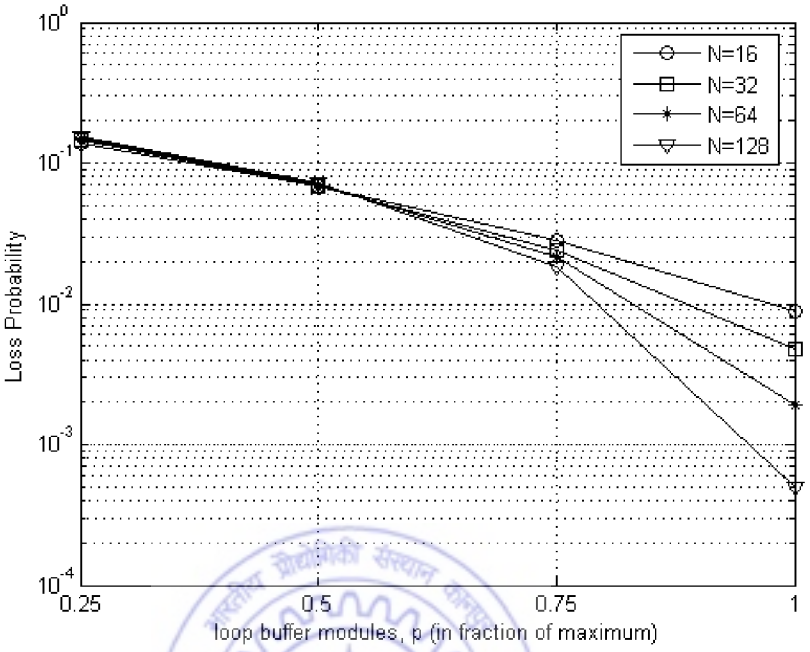


Figure 5.6: Total number of modules in each case is M $(= p \times N/D)$ and buffer capacity equals to MB at $B = D = 4$ and $\rho = 0.7$.

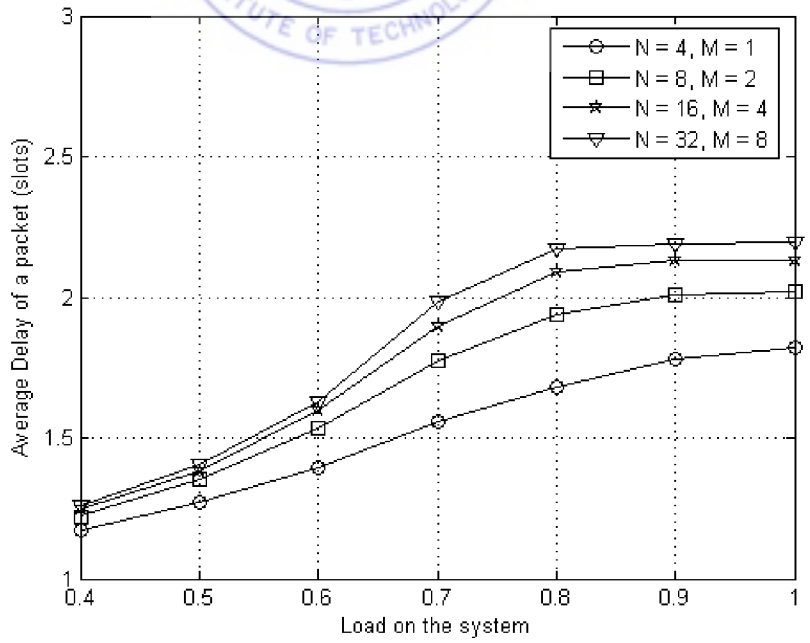


Figure 5.7: Number of module is maximum for each case at $B = 4$.

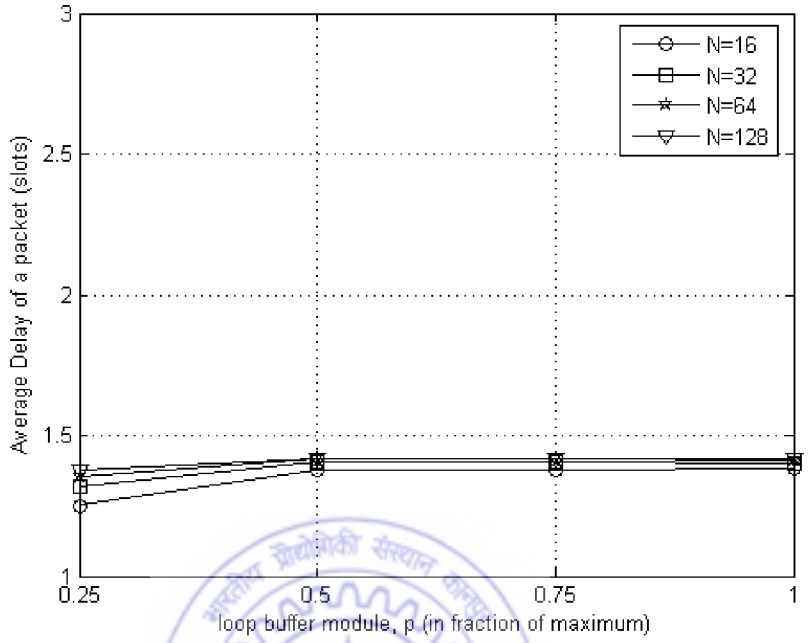


Figure 5.8: Total number of modules in each case is M $(= p \times N/D)$ and buffer capacity equals to MB at $B = D = 4$ and $\rho = 0.5$.

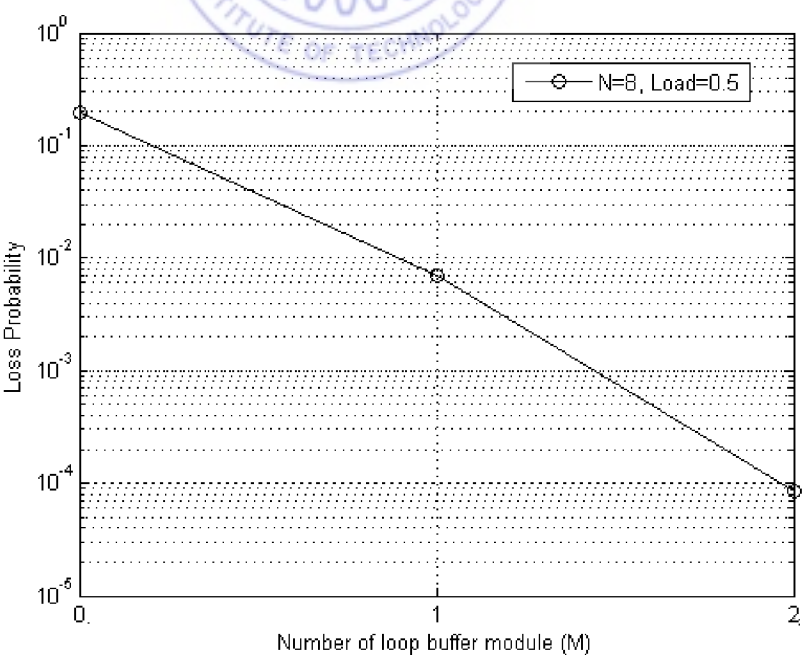


Figure 5.9: Total buffer capacity is equal to MB at $B = 4$.

5.4 Switch with circulation limit

The loop buffer modules used in the switch, comprise of several optical components. These components will degrade the signal quality during recirculations, and may increase the bit-error rate (BER). This degradation will impose a limit on the number of circulations performed by any packet, in order to be stored in the loop buffer module. In this section, the effects of circulation limit on previous results are discussed. Also, the crosstalk has not been considered in the following analysis.

5.4.1 Power Budget Analysis

The proposed switch is analyzed in terms of loss, power and noise by using the model shown in Figure 5.10. This analysis has been done to find the circulation limit (C) which is then used as the parameter for the scheduling algorithm.

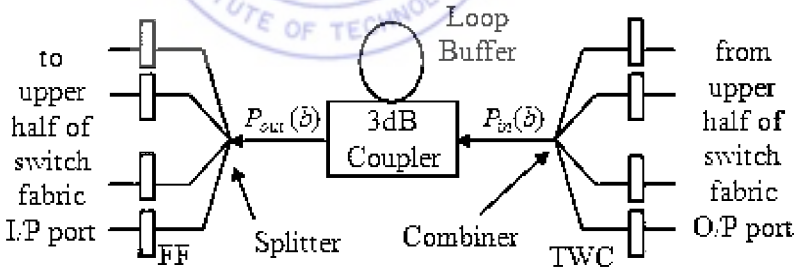


Figure 5.10: Model of Loop Buffer Memory Module.

5.4.1.1 Loss Analysis

For the convenience of calculations, the loss in this architecture has been divided into three parts.

1. The input section of the buffer module consists of TWC and combiner. Hence the loss from switch input up to the loop buffer input, termed as Insertion loss (A_{ins}), is given as

$$A_{ins} = L_{SS}L_{TWC}L_{Com} \tag{5.4.7}$$

2. Loss through the loop buffer is termed as Recirculation loss (A_{re}). This has been obtained by breaking the loop (Figure 5.3) in two parts for the ease of calculation. These are defined as below,

$$A_1 = L_{3dB}L_{DEMUX}L_{TWC}L_{Com}6L_SL_{F1} \tag{5.4.8}$$

$$A_2 = L_{ISO}4L_SL_{F2} \tag{5.4.9}$$

where A_1 is the loss from entry port of loop buffer up to the input of EDFA and A_2 is the loss after EDFA up to 3dB coupler. These variables are defined in Table 5.1 with relevant values. Total loss of the loop buffer after one circulation can be given as $A_L = (A_1A_2)$. Hence after K circulations, the Recirculation loss will be $A_{re} = (A_L)^K$.

3. The output section of the buffer module consists of splitters and FFs. So the loss from the loop buffer output up to the switch output, termed as Extraction loss (A_{ext}), is given as

$$A_{ext} = L_{SP}L_{FF}L_{SS} \tag{5.4.10}$$

Thus the total loss through the switch architecture, after performing K circulations, is

$$A = A_{ins}A_{re}L_{3dB}A_{ext} \tag{5.4.11}$$

The term L_{3dB} is again inserted in the Equation 5.4.11 because the packet passes through the 3dB coupler for one more time (i.e., $K + 1$ times) when it leaves the loop.

Symbol	***Parameter***	***Value***
R	Responsivity	1.28 Amp/Watts
n_{sp}	Population inversion factor	1.2
h	Planck's Constant	6.6×10^{-34} J-s
c	Speed of light	3×10^{8} m/s
B_e	Electrical Bandwidth	10 GHz
B_o	Optical Bandwidth	20 GHz
q	electronic charge	1.6×10^{-19} Coulomb
ϵ	Extinction Ratio	∞
R_L	Load Resistance	300 Ω
T	Temperature	300 K
K_B	Boltzmann constant	1.38×10^{-23} J/K
L_{3dB}	3dB coupler Loss	3.4 dB
L_{Com}	Combiner Loss ($W \times 1$)	$10(\text{Log}_{10}\text{W})$ dB
L_{SP}	Splitter Loss ($1 \times W$)	$10(\text{Log}_{10}\text{W})$ dB
L_{DEMUX}	DEMUX Loss ($1 \times W$)	$1.5(\text{Log}_2\text{W-1})$ dB
L_{TWC}	TWC Loss	2 dB
L_{FF}	Fixed Filter Loss	1 dB
L_S	Splice Loss	0.2 dB
$L_{F1} = \text{L}_{F2}$	Fiber Loss	0.2 dB/Km
L_{ISO}	Isolator Loss	0.15 dB
L_{BPF}	Band Pass Filter Loss	1.0 dB
L_{SS}	Space Switch Loss ($N \times N$)	$0.5(\text{Log}_2\text{N})$ dB
Γ	Confinement Factor	1
γ	Scattering Loss	1000/m
P_p	Pump Power	10 mW

Table 5.1: Value of Different Parameters

5.4.1.2 Power Analysis

The TWC is a noisy device i.e., it adds noise to the incoming signal whenever it performs wavelength conversion; while it will not introduce any noise, when it remains

transparent (no wavelength conversion). But, the TWC is sometimes considered as noiseless device, during conversion process, for the performance analysis because the introduction of noise may be reduced by the regeneration of the signal inside the TWC [42]. So, we have done the analysis in both ways i.e., considering: i) TWC as a noiseless device and ii) TWC as a noisy device.

1. TWC as a noiseless device

If we follow the above model (Figure 5.10) then the power of bit '1' and bit '0', entering through the input of loop, are

$$P_{in}(1) = P_{av}A_{ins}\left(\frac{2\epsilon}{1+\epsilon}\right) \tag{5.4.12}$$

and

$$P_{in}(0) = P_{av}A_{ins}\left(\frac{2}{1+\epsilon}\right) \tag{5.4.13}$$

where P_{av} is average signal power at the switch input, and 'ϵ' is the extinction ratio defined as $\epsilon = [P(1)/P(0)]$. Thus the signal power after one circulation, just before the 3dB coupler, is given by

$$P_1(b) = A_L P_{in}(b)G + (G-1)n_{sp}h\nu B_o A_2 \tag{5.4.14}$$

Here $b = 1$ for bit '1' and 0 for bit '0'. In the Equation 5.4.14, the first term represents the signal power and the second term represents amplified spontaneous emission (ASE) noise power [47]. Here, A_L is the loss of the loop in one circulation, G is the gain of EDFA and B_o is the optical bandwidth.

The power for bit 'b' after 2 circulations, just before the 3dB coupler, is

$$P_2(b) = A_L P_1(b) G + (G-1) n_{sp} h\nu B_o A_2 \tag{5.4.15}$$

In the above equation, replacing the value of $P_1(b)$ from Equation 5.4.14, the expression of $P_2(b)$ will be changed as,

$$P_2(b) = (A_L)^2 P_{in}(b) (G)^2 + (G-1) n_{sp} h\nu B_o A_2 (1 + A_L G) \tag{5.4.16}$$

Similarly, the expression after 3 circulations will be

$$P_3(b) = (A_L)^3 P_{in}(b) (G)^3 + (G-1) n_{sp} h\nu B_o A_2 [1 + A_L G + (A_L G)^2] \tag{5.4.17}$$

Thus, the power for bit 'b' after K circulations, just before the 3dB coupler, is

$$\begin{aligned} P_K(b) &= (A_L)^K P_{in}(b) (G)^K + \\ &\quad (G-1) n_{sp} h\nu B_o A_2 [1 + A_L G + (A_L G)^2 + \ .\ .\ + (A_L G)^{K-1}] \end{aligned} \tag{5.4.18}$$

We can also write the term $P_K(b)$ as,

$$P_K(b) = (A_L)^K P_{in}(b) G^K + (G-1) n_{sp} h\nu B_o A_2 F \tag{5.4.19}$$

where

$$F = 1 + A_L G + (A_L G)^2 + \ .\ .\ + (A_L G)^{K-1} \tag{5.4.20}$$

or

$$F = \begin{cases} \frac{1-(A_L G)^K}{1-A_L G}, & A_L G < 1 \\ K, & A_L G = 1 \end{cases} \tag{5.4.21}$$

We have not considered the case of $A_L G > 1$ because under this condition, the fiber loop buffer will start behaving like an oscillator and finally, starts to lase. To achieve maximum SNR, the product of loop gain and loop loss must be equal to unity [45] i.e., $A_L G = 1$. Therefore,

$$P_K(b) = P_{in}(b) + K(G-1)n_{sp}h\nu B_o A_2 \tag{5.4.22}$$

Thus the power at the output of loop will be

$$P_{out}(b) = P_K(b)L_{3dB} \tag{5.4.23}$$

Finally, the power for bit 'b' at the output of the switch is given as,

$$P(b) = P_{out}(b)A_{ext} \tag{5.4.24}$$

2. TWC as a noisy device

In this section, we have considered the TWC as a noisy device and taken the TWC model as given in [35]. As long as the packets circulate inside loop, the corresponding TWC will remain transparent i.e., the packets will keep on circulating at their respective wavelength. Since, the tuning is not required, so the TWC will not induce any noise. The noise added in the signal due to the conversion process in TWC (given by Sabella, et. al. in [35]) is

$$n_{sp}(G_c - 1)h\nu\left(\frac{\Gamma g(0)}{\Gamma g(0) - \gamma}\right) \times \left(1 + \frac{\chi}{G_c} + \frac{\chi P_s}{P_p G_c}\right) \tag{5.4.25}$$

We have modified this noise expression according to our switch architecture. In our case, the power out of the TWC is $L_{TWC}P_{av}$ instead of P_{in}. Before entering to the loop

buffer, the above noise will also suffer additional losses of L_{Com} due to the presence of the combiner at the loop input. Also, during the read-out/write-in process, the TWC will be tuned accordingly and thus, it will introduce the noise into the signal power. Hence, the modified expression of the power for bit '1' (as compared to Equation 5.4.12), entering the loop buffer, will be given as

$$P_{in}(1) = P_{av}A_{ins}\left(\frac{2\epsilon}{1+\epsilon}\right) + n_{sp}(G_c-1)h\nu\left(\frac{\Gamma g(0)}{\Gamma g(0)-\gamma}\right)\times \left(1+\frac{\chi}{G_c}+\frac{\chi P_{av}L_{TWC}}{P_pG_c}\right)L_{Com}B_o \quad (5.4.26)$$

The second term in the Equation 5.4.26 is the noise added by TWC during conversion process. This term is added because whenever the packet is scheduled to be stored in the buffer, it will be passed through one of the D TWCs, placed at the input of buffer module. Then the tuning is performed to allocate the free buffer wavelength. Here G_c is the gain of SOA used inside the TWC. The terms G_c and $g(0)$ are obtained solving the set of equations given in [35]. Conversion efficiency (χ) is assumed to be 1 in the calculations. Other parameters and their values are defined in Table 5.1. For bit '0', the TWC does not contribute any noise term, so its power expression will remain same as given in Equation 5.4.13.

During the recirculation in the loop, if the number of maximum allowed circulations is K, then the TWC placed inside the loop will perform tuning only in the K^{th} circulation (for worst case scenario). Thus in this condition, the TWC will not be tuned till $(K-1)^{th}$ circulations, and the power for bit 'b' after $(K-1)$ circulations will be

$$P_{K-1}(b) = P_{in}(b) + (K-1)(G-1)n_{sp}h\nu B_oA_2 \quad (5.4.27)$$

The above power will enter TWC during the K^{th} revolution, and now the TWC noise

will be added to it because of tuning. The new term for power after K circulations will be given as

$$\begin{aligned} P_K(b) &= P_{in}(b) + n_{sp}(G_c - 1)h\nu \left(\frac{\Gamma g(0)}{\Gamma g(0) - \gamma}\right) \times \\ &\qquad \left(1 + \frac{\chi}{G_c} + \frac{\chi P_{K-1}(b) L_{3dB} L_{DEMUX} L_{TWC}}{P_p G_c}\right) L_{Com} B_o G A_2 \\ &\quad + K(G-1) n_{sp} h\nu B_o A_2 \end{aligned} \tag{5.4.28}$$

Hence, the final output power for bit 'b' is shown as

$$P(b) = P_K(b) L_{3dB} A_{ext} \tag{5.4.29}$$

5.4.1.3 Noise Analysis

The optical amplifiers not only amplify the signal but also add amplified spontaneous emission (ASE) noise to the signal. The square law detection by the photodetector of the receiver generates various intermodulation noise components. These noise components are shot noise, ASE-ASE beat noise, sig-ASE beat noise, ASE-shot beat noise and thermal noise with variances given by σ_s^2, σ_{sp-sp}^2, σ_{sig-sp}^2, σ_{s-sp}^2 and σ_{th}^2 respectively [47]. These noise variances for bit 'b', after performing K circulations, are given by

$$\sigma_s^2 = 2qRP(b)B_e \tag{5.4.30}$$

$$\sigma_{sp-sp}^2 = R^2 P_{sp}^2(K)(2B_o - B_e)\frac{B_e}{B_o^2} \tag{5.4.31}$$

$$\sigma_{sig-sp}^2 = 4R^2 P(b)\frac{P_{sp}(K)B_e}{B_o} \tag{5.4.32}$$

$$\sigma_{s-sp}^2 = 2qRP_{sp}(K)B_e \quad and \tag{5.4.33}$$

$$\sigma_{th}^2 = \frac{4kTB_e}{R_L} \tag{5.4.34}$$

Here, $P_{SP}(K)$ is the spontaneous noise power and is given by

$$P_{sp}(K) = K(G-1)n_{sp}h\nu B_o A_2 L_{3dB} A_{ext} \tag{5.4.35}$$

In the Equation 5.4.35, the TWC is considered as a noiseless device. Now, If we consider the TWC as a noisy device, then the Equation 5.4.35 will be changed, and the new expression will be obtained from Equation 5.4.28 as,

$$P_{sp}(K) = [P_K(b) - P_{in}(b)]L_{3dB} A_{ext} \tag{5.4.36}$$

The total noise variance for bit 'b' is

$$\sigma^2(b) = \sigma_s^2 + \sigma_{sp-sp}^2 + \sigma_{sig-sp}^2 + \sigma_{s-sp}^2 + \sigma_{th}^2 \tag{5.4.37}$$

The bit-error rate [47] can be obtained as

$$BER = Q\left(\frac{I(1) - I(0)}{\sigma(1) - \sigma(0)}\right) \tag{5.4.38}$$

where $Q(x)$ is known as the error function and is defined as

$$Q(z) = \frac{1}{\sqrt{2\pi}} \int_z^\infty exp(-z^2/2)dz \tag{5.4.39}$$

The terms $I(1) = RP(1)$ and $I(0) = RP(0)$ are photocurrent, sampled by the receiver during bit '1' and bit '0' respectively, and R is the responsivity of photodetector.

5.4.1.4 Calculation

We have used the model given in [24] for calculation of the gain of the EDFA. The number of channels passing through EDFA will vary during different time slots, and this

will change the gain of the EDFA. Thus, the function of automatic gain control (AGC) scheme has been assumed where the gain of EDFA will remain constant irrespective of the number of channels passing through it [45, 52]. The length as well as the gain of EDFA is considered as to maintain the condition of unity loop gain for a signal inside the loop (i.e., $A_L G = 1$), for various values of buffering capacity (i.e., $B = 4$, 8 and 16). The gain of the EDFA for different buffer space has been computed by considering the loss through each component of the loop, while the corresponding doped fiber lengths have been taken from [24] and are shown in Table 5.2.

The length of the loop is equal to the distance covered by light in a packet duration, and it is given by $L = cb'/nR_b$, where c is the speed of light, b' is the number of bits, n is the refractive index of fiber and R_b is the bit rate. The value of n is taken as 1.55. We have assumed equal length packets of 53 *bytes* alongwith 1 *byte* period of guard time on each side. This length is plotted against bit rate in Figure 5.11. The minimum loop length should be equal to the length of the EDFA, in order to provide the sufficient gain. We can observe in Table 5.2 that the minimum length of fiber is 10m which is needed to maintain the gain of 16.85dB at B = 4. It is obvious from Figure 5.11 that the maximum bit rate, which can be used, is 8Gbps for 10m length of fiber. Similarly for $G = 26.65$dB at $B = 16$, the required minimum fiber length is 14m and thus, the corresponding maximum bit rate will be 6Gbps. If we consider a bit rate of 5Gbps (common for all three cases of B), the required loop length will be

B	**G**	**Length of EDFA**
4	16.85 dB	10 m
8	21.75 dB	11 m
16	26.65 dB	14 m

Table 5.2: Length of the EDFA to provide the required gain

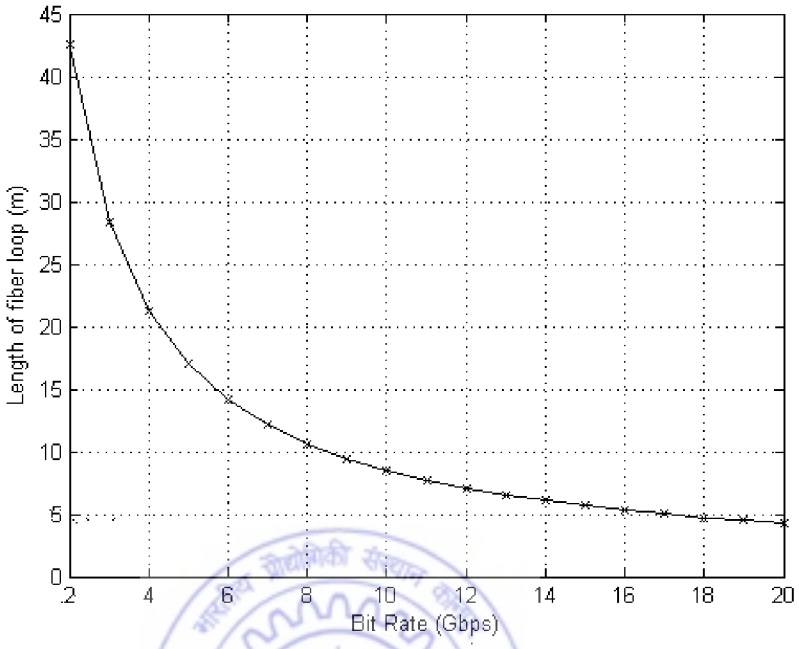


Figure 5.11: Variation of loop length with data rate

17.04m. Since the EDFA length should be 10m for $B = 4$, the required fiber length will be 7.04m to construct the complete delay loop of 17.04m.

The wavelength selection has been done by following the ITU-T grid and the chosen range of wavelength is from 1550.12nm to 1552.52nm with a spacing of 0.8nm (Δf = 100GHz) for $B = 4$. To minimize the crosstalk, channel spacing should be greater than 6 times the bit rate (i.e., $\Delta f \geq 6R_b$) [39, 73]. Since the channel spacing (Δf) is considered equal to 100GHz, and the selected bit rate (R_b) is 5Gbps, so we can ignore the effect of crosstalk as it satisfies the above mentioned condition i.e., $\Delta f > 6R_b$ because $6R_b$ = 30Gbps.

We have obtained the number of maximum allowed circulations (C) at different values of power levels (in mW) with various combinations of switch sizes (N) and number of buffer wavelengths (B) (Table 5.3). The value of C is the largest value of K

(circulations count) for which $BER \leq 10^{-9}$ (if the signal is detected). It is found in the computed results that if we increase B beyond D then the number of maximum allowed circulations decreases (Table 5.4) which may degrade the performance of a large switch drastically. Hence the maximum number of possible wavelengths in any of the buffer modules is chosen as 4 because for larger values of B (i.e., 8 and 16), the number of allowed circulations are insufficient for all power levels. We have also calculated the number of maximum allowed circulations considering the TWC as the noisy device and the data is given in Table 5.5 for $B = 4$. If we compare these data with that one given in Table 5.3, then we can observe that there is not much effect of TWC noise on the number of maximum allowed circulations. So, the results for loss probability will be nearly the same for both the cases.

N	**B**	**C at P=1mW**	**C at P=2mW**	**C at P=5mW**	**C at P=10mW**
16		2	5	13	26
32		2	4	10	20
64	4	1	3	8	16
128		1	2	6	13
256		0	2	5	10
16		0	1	3	7
32		0	1	3	6
64	8	0	0	2	4
128		0	0	1	3
256		0	0	1	3
16		0	0	1	2
32		0	0	1	2
64	16	0	0	0	1
128		0	0	0	1
256		0	0	0	1

Table 5.3: Maximum number of allowed circulations (C) for various sizes of core switch ($2N$) and buffer wavelength (B) at different power levels (P) for $D = 4$, considering TWC as the noiseless device

D	**B**	**C at P=1mW**	**C at P=2mW**	**C at P=5mW**	**C at P=10mW**
4	4	2	5	13	26
4	8	0	1	3	7
8	8	0	0	0	1

Table 5.4: Maximum number of allowed circulations (C) for switch of size $N = 16$ and for various values of D and B at different power levels

N	**B**	**C at P=1mW**	**C at P=2mW**	**C at P=5mW**	**C at P=10mW**
16		2	4	12	25
32		1	3	10	20
64	4	1	2	7	16
128		0	2	6	12
256		0	1	4	10

Table 5.5: Maximum number of allowed circulations (C) for various sizes of core switch ($2N$) at different power levels (P) for $D = 4$, considering TWC as the noisy device

5.4.2 Scheduling algorithm

The circulation limit will act as a special case of buffering limit. In other words, if the packets are allowed to take maximum C circulations then, not more than C packets for any single output can be stored in the buffer. This is due to the reason that the $(C + 1)^{th}$ packet stored in buffer module, has to take $C + 1$ revolutions in the loop before its delivery to the intended output. Hence, the correct reception of that packet will not be possible because the obtained BER at the output, will become more than the acceptable level.

The number of steps for applying scheduling algorithm in this case will be same as given in section 5.3.1, but with some limitation imposed on the storing of packets in the buffer. The modification is done only in constraint 1, while the second constraint

and the rest of the steps of that algorithm remain same. The modified constraint 1 is given below:

1. (*Modified constraint 1*) The number of buffered packets (x_j) for the output j should never be greater than the maximum buffering capacity or the circulation limit i.e., $x_j \leq min(MB, C)$ for $1 \leq j \leq N$.

The simulations have been done using this modified constraint in addition to the scheduling algorithm given in section 5.3.1, and the results are discussed in following section.

5.4.3 Performance Analysis and Results

The simulation of the proposed switch with circulation limit has been done to estimate the '*packet loss probability*' and '*average packet delay*' under various loading conditions. The switch performance has been investigated for different number of buffer modules (M) and the number of maximum allowed circulations (C) at different power levels. The results are used to determine the values of parameters for optimal operation. Figure 5.12 to 5.14 show results of packet loss probability for the switch of size $2N = 32$ where, as defined earlier, 16 of 32 ports are the actual inputs and other 16 ports are used to connect different number of buffer modules. We can observe in Figure 5.12 that as the signal power increases, the probability of packet loss decreases. This happens due to the increment in C with signal power. But this increment in power level beyond a certain value does not give any further advantage because the value of C at such power level will become greater than $M \times B$ (Table 5.3), and the buffering will be limited to $min(MB, C)$ for all such power levels. Hence the packet loss probability is almost

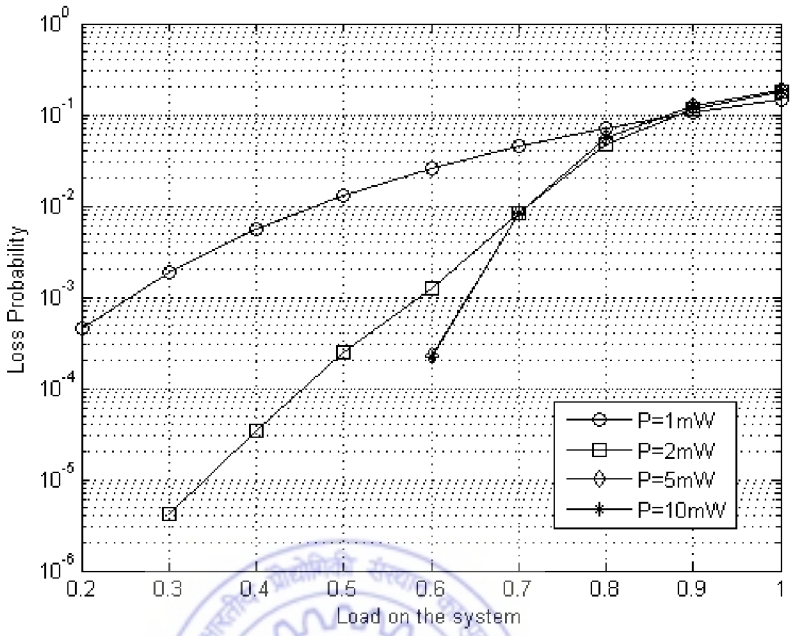


Figure 5.12: Probability of packet loss with Load on the system for $N = 16$, $M = 4$ at different values of signal power (P).

same for $P = 5$ and $10mW$, as for these values, the buffering limit will be 13 and 16 respectively due to the circulation limit. It has been observed that as the number of buffer modules (M) increases, packet loss probability decreases (Figure 5.13 and 5.14). These results hold for $B = D = 4$.

The average delay performance for the switch of size $2N = 32$ is shown in Figure 5.15 to 5.17. It is clear from these plots that the delay increases with the number of modules. Also, it remains nearly same for $P = 5$ and $10mW$ because of the circulation limit. This indicate that in case of $P = 10mW$, although the packet can be stored for 26 slots (Table 5.3) but due to the maximum buffering limitation, the packet cannot be circulated more than 16 slots. Thus the optimized result for $N = 16$ are achieved at $B = D = 4$, $P = 5mW$ and $M = 4$.

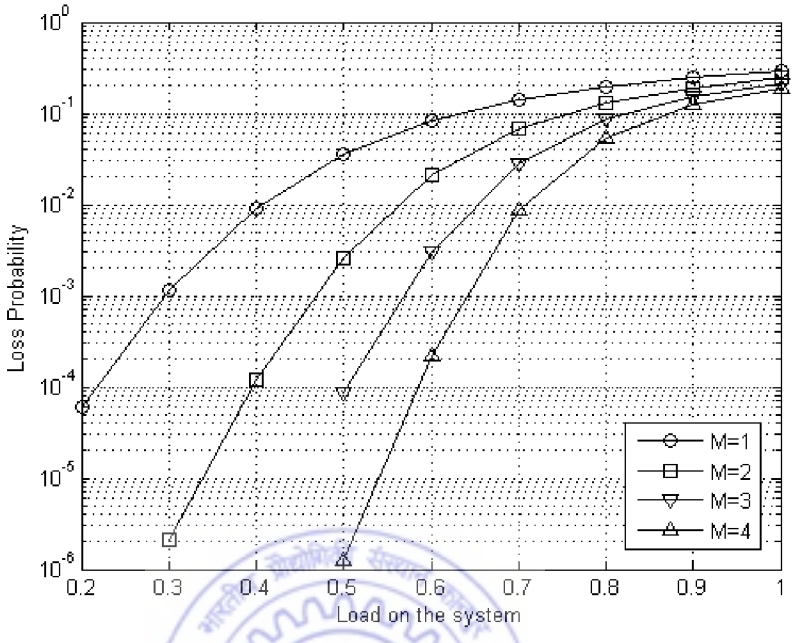


Figure 5.13: Probability of packet loss with Load on the system for $N = 16$, $P = 5mW$ at different values of number of buffer modules (M).

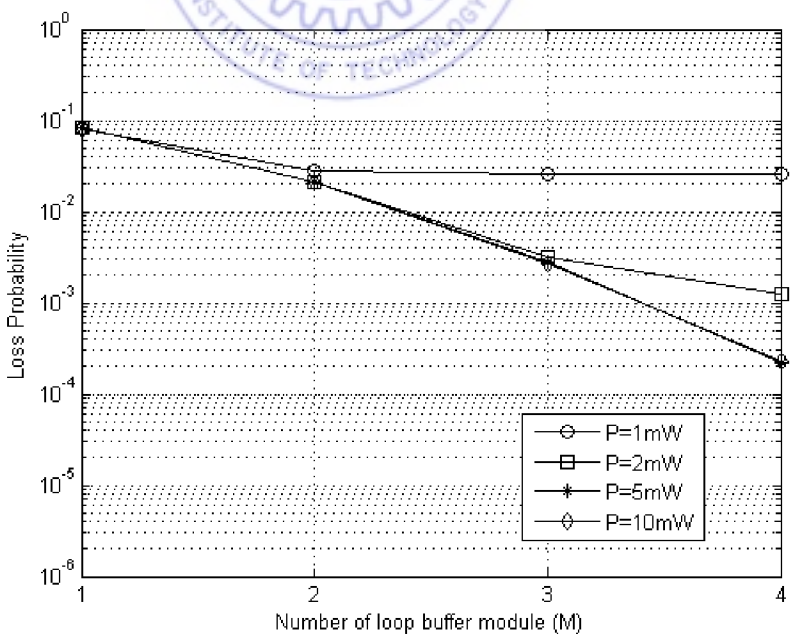


Figure 5.14: Probability of packet loss with number of buffer module (M) for $N = 16$, $\rho = 0.6$ at different values of signal power (P).

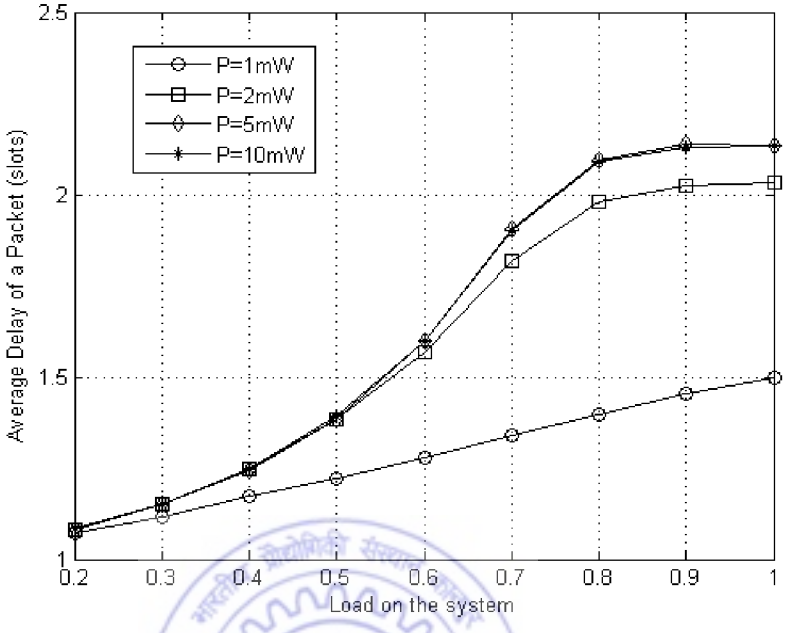


Figure 5.15: Average Delay with Load on the system for $N = 16$, $M = 4$ at different values of signal power (P).

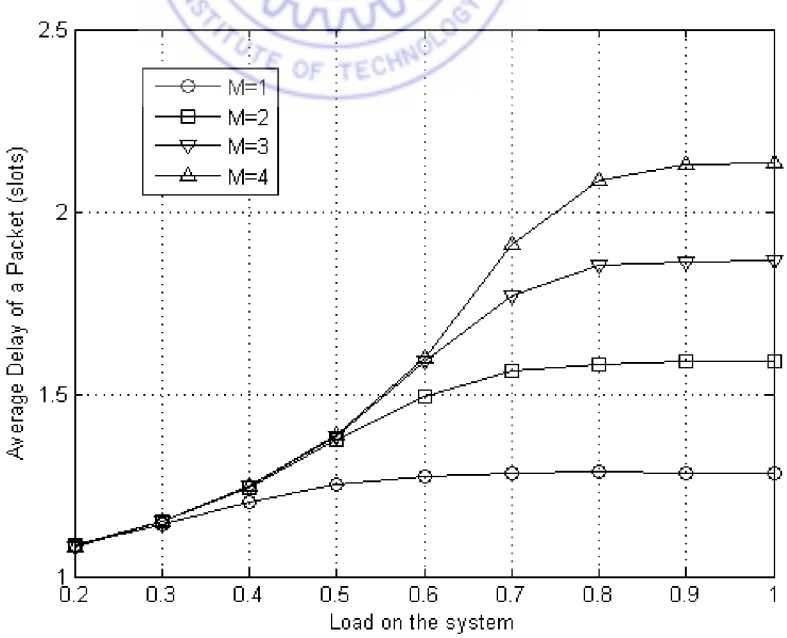


Figure 5.16: Average Delay with Load on the system for $N = 16$, $P = 5mW$ at different numbers of module (M).

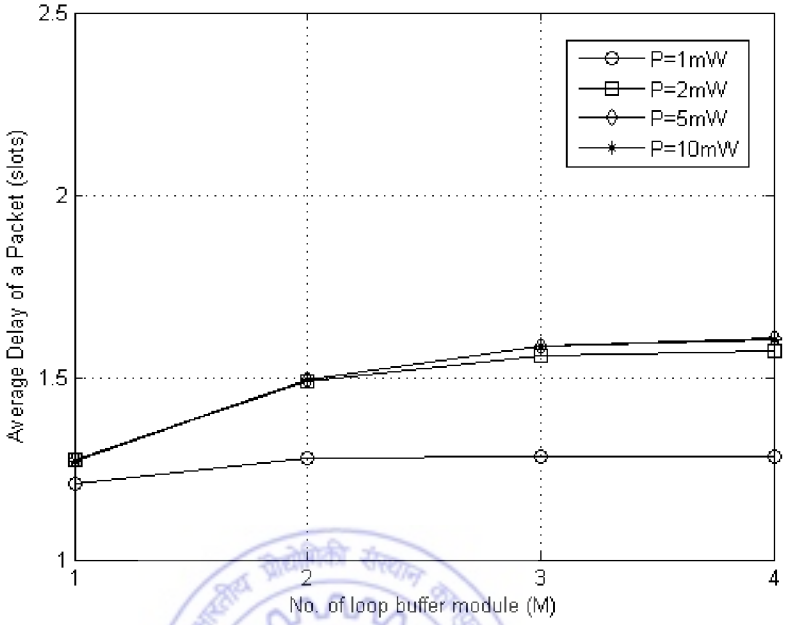


Figure 5.17: Average Delay with number of buffer module (M) for $N = 16$, $\rho = 0.6$ at different values of signal power (P).

5.4.3.1 *Effect of noisy TWC*

The results shown till now are based on the assumption that the TWC is a noiseless device. We have also done the performance analysis considering the TWC noise. We have found $C = 2, 4, 12$ & 25 for the noisy TWC (Table 5.5) at $P = 1, 2, 5$ & $10mW$ and $N = 16$ while $C = 2, 5, 13$ & 26 for the noiseless case of TWC (Table 5.3). There is not much difference among the numbers of maximum allowed circulations at various power levels. The comparative results for packet loss probability and average delay are shown in Figure 5.18 and 5.19 respectively. We observe that the results at all the power levels are overlapping except the case of $P = 2mW$ where the loss probability is better and the average delay is more for the case of noiseless TWC. This will happen because the case of $C = 4$ at $P = 2mW$ for noisy TWC may reject some more packets when the total capacity is 16 ($= MB$) as compared to the case of $C = 5$ for noiseless TWC.

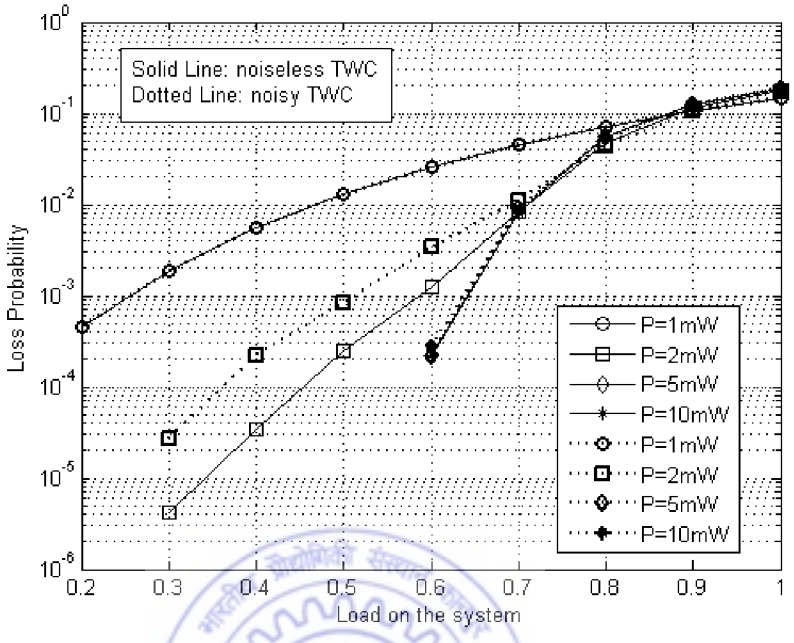


Figure 5.18: Comparative results for Probability of packet loss at $N = 16, B = 4, M = 4$ (noiseless TWC vs. noisy TWC).

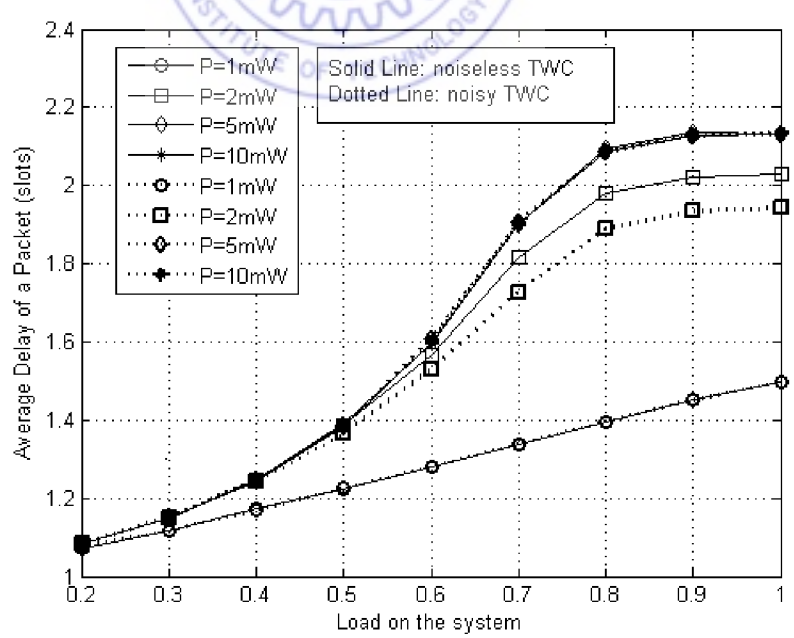


Figure 5.19: Comparative results for Average Delay at $N = 16, B = 4, M = 4$ (noiseless TWC vs. noisy TWC).

5.5 Mathematical Analysis

In order to verify the simulator, we have taken a computational model [56] and modified it accordingly to represent our switch. By comparing the computational results with simulation, we will verify the correctness of the simulation method.

The packets are assumed to be randomly arriving with uniform rate. Depending upon the number of packets arriving and the number of busy output ports, various buffer states can be attained. The state of the buffer is described by a vector 'b' of positive integers and of length N i.e., $b = (b_1, b_2, ...b_N)$ for $1 \leq i \leq N$. The term b_i represents the buffer state element for the i^{th} output and its value (storage capacity) ranges from 0 to $min(MB, C)$. The sum of packets in any of the buffer state b will be less than or equal to MB i.e., $\sum b_i \leq MB$. As defined earlier, M is the number of module used in the architecture, B represents the total buffering capacity of each module, and C is the circulation limit for any packet. Thus, $min(MB, C)$ will be used as the maximum buffering capacity for individual output and MB will be the maximum buffer capacity of whole switch. The maximum value of MB will always be equal to N, since we have assumed $B = D$ for each loop buffer module.

Depending upon the arrival pattern during every slot, there will be transitions between the buffer states. Each possible arrival pattern is described by a vector of length N i.e., $I = (I_1, I_2, ...I_N)$ where the value of each element I_i represents the number of packets arriving for the i^{th} output during that time slot. The total number of packets that can arrive during any time slot will not be more than N (i.e., $\sum I_i \leq N$). For a given buffer state b and the arrival pattern I, the new buffer state will be an N length

vector $d = (d_1, d_2, ...d_N)$ where

$$d_i = \begin{cases} 0, & b_i = 0,\ I_i = 0 \\ b_i + I_i - 1, & b_i + I_i - 1 \leq min(Z, C) \\ min(Z, C), & otherwise \end{cases} \tag{5.5.40}$$

with

$$Z = \begin{cases} MB - \sum_{j=1}^{i-1} d_j - \sum_{j=i}^{N} R(b_j), & i > 1 \\ MB - \sum_{j=i}^{N} R(b_j), & i = 1 \end{cases} \tag{5.5.41}$$

and

$$R(b_j) = \begin{cases} b_j - 1, & b_j > 0 \\ 0, & b_j = 0 \end{cases} \tag{5.5.42}$$

Here, $R(b_j)$ is the number of packets for output j, left in buffer during the current time slot. The above formulation assumes sequential scanning i.e., the packets at lower indexed input are given priority while buffering. This assumption is justified as we are not biased towards any particular input/output, but we are interested in the overall performance of the switch.

The available buffer space after completion of any time slot will be equal to T and is defined as

$$T = MB - \left(\sum_{i=1}^{N} b_i - \Delta \right) \tag{5.5.43}$$

where Δ is the count of all those output ports for which there is at least one packet in the buffer, and is defined as

$$\Delta = \sum_{j=1}^{N} \delta_b(j) \tag{5.5.44}$$

and

$$\delta_b(j) = \begin{cases} 0, & b_j = 0 \\ 1, & b_j > 0 \end{cases} \tag{5.5.45}$$

If the number of packets arriving during any time slot will be greater than T, then the packet destined for at least one of the output ports will be dropped. The reason is that, either the individual buffer limit for that output or the maximum buffer limit for whole switch is achieved. For a given N, the total number of feasible input patterns (IP) will be given by

$$IP = \sum_{k=0}^{N} {}^{N+k-1}C_k \tag{5.5.46}$$

where k is the total number of packets arriving in a slot. The term '*feasible*' is used here to indicate that only those input patterns are considered where $I_i \leq N$ and $\sum I_i \leq N$ for $1 \leq i \leq N$. The vale of IP for various N is given in Table 5.6. The induction proof for the above expression of IP is given in the next sub-section.

Similarly, the total number of feasible buffer states (BS) will be calculated as

$$BS = \sum_{k=0}^{MB} {}^{N+k-1}C_k \tag{5.5.47}$$

considering $b_i \leq MB$ and $\sum b_i \leq MB$. Here, those values of MB are taken which will optimize the performance of the switch. Till now the value of BS does not consider the circulation limit. Now considering the circulation limit, the new value of BS will be

$$BS' = BS - \sum_{i} (states\ with\ b_i > min(MB, C)) \tag{5.5.48}$$

Here, The values of IP and BS are equal because $N = MB$ is considered for this switch. Their value increase drastically with N (Table 5.6). Also, $BS' \leq IP$ but still

N	IP (=BS)
4	70
8	12870
16	601080390

Table 5.6: Feasible number of input pattern (IP) for switch of size N

BS' will be very large in number and it may not be possible to obtain the mathematical results for a large switch. So, we will show the comparative results (mathematical versus simulation) for a smaller switch of size $N = 4$.

5.5.1 Induction Proof of the Formula for Input Pattern (IP)

Considering the case of $N = 4$. The number of packets that can arrive for a particular output port is 0, 1, 2, 3, and 4. Mathematically, this probability can be stated as,

$$P_o = (1 + x + x^2 + x^3 + x^4)^4 \tag{5.5.49}$$

Expanding the above equation and collecting the terms having coefficient less than or equal to 4. We get,

$$\begin{aligned} P_o = {} & {}^4C_0 + {}^4C_1(1 + x + x^2 + x^3 + x^4) + {}^4C_2(x^2 + 2x^3 + 3x^4) + \\ & {}^4C_3(x^3 + 3x^4)^4 + {}^4C_4(x^4) \end{aligned} \tag{5.5.50}$$

Now considering the coefficient of x^0, x^1, x^2, x^3 and x^4 as

$$\begin{aligned} P(0) &= {}^4C_0 \\ P(1) &= {}^4C_1 \\ P(2) &= {}^4C_1 + {}^4C_2 \\ P(3) &= {}^4C_1 + 2 \times {}^4C_2 + {}^4C_3 \\ P(4) &= {}^4C_1 + 3 \times {}^4C_2 + 3 \times {}^4C_3 + {}^4C_4 \end{aligned}$$

Total number of Input Patterns (IP) when 0 packet arrive,

$$IP_0 = P(0) = {}^4C_0$$

Total number of Input Patterns (IP) when at most 1 packet arrives,

$$IP_1 = P(0) + P(1) = {}^4C_0 + {}^4C_1$$

Total number of Input Patterns (IP) when at most 2 packets arrive,

$$IP_2 = P(0) + P(1) + P(2) = {}^4C_0 + 2 \times {}^4C_1 + {}^4C_2 = {}^4C_0 + {}^4C_1 + {}^5C_2$$

Similarly, the total number of Input Patterns (IP) when at most 3 packets arrive,

$$IP_3 = P(0) + P(1) + P(2) + P(3) = {}^4C_0 + {}^4C_1 + {}^5C_2 + {}^6C_3$$

Total number of Input Patterns (IP) when at most 4 packets arrive,

$$IP_4 = P(0) + P(1) + P(2) + P(3) + P(4) = {}^4C_0 + {}^4C_1 + {}^5C_2 + {}^6C_3 + {}^7C_4$$

Since, the result will be similar for ${}^4C_0$ and ${}^3C_0$, as both will take the value 1, the above expression for IP_4 can be made more meaningful by replacing ${}^4C_0$ with ${}^3C_0$. Thus,

$$IP_4 = P(0) + P(1) + P(2) + P(3) + P(4) = {}^3C_0 + {}^4C_1 + {}^5C_2 + {}^6C_3 + {}^7C_4$$

Now writing this equation in the generalized form,

$$IP = P(0) + P(1) + P(2) + ... + P(k) = {}^{N-1}C_0 + {}^{N}C_1 + {}^{N+1}C_2 + ... + {}^{N+k-1}C_k$$

Thus, the total number of Input Pattern for any N will be

$$IP = \sum_{k=0}^{N} {}^{N+k-1}C_k \tag{5.5.51}$$

5.5.2 Comparison of Mathematical and Simulation Analysis

We have verified the simulation results with the computational one given in [56] where results are shown for a large range of individual as well as total buffer length values. For verification, we will consider the result of packet loss probability for the case of $N = 4, M = 1, B = 4$. For this configuration, the architectural logic of proposed switch will be nearly similar to that one presented in [56]. In the proposed architecture, we have considered the circulation limit (C) for packets stored in the buffer which will in turn, limit the individual buffer capacity. We have shown the value of C for large switches ($N \geq 16$) in the Table 5.3, and it indicates that C will be larger than MB for $N = 4, M = 1, B = 4$ at all power levels considered for simulations. Thus, there will not be any limit on the number of circulations because the net individual buffer capacity will be MB because of $min(MB, C)$. Hence, for verification of the simulation

result by taking care of the circulation limit, we have considered a hypothetical value of $C = 2$ for $N = 4$ and compared the obtained result of packet loss probability with the one given in [56]. The comparative results are shown in Figure 5.20. It is found that the variation of packet loss probability, obtained from simulation method, closely follows the mathematical analysis.

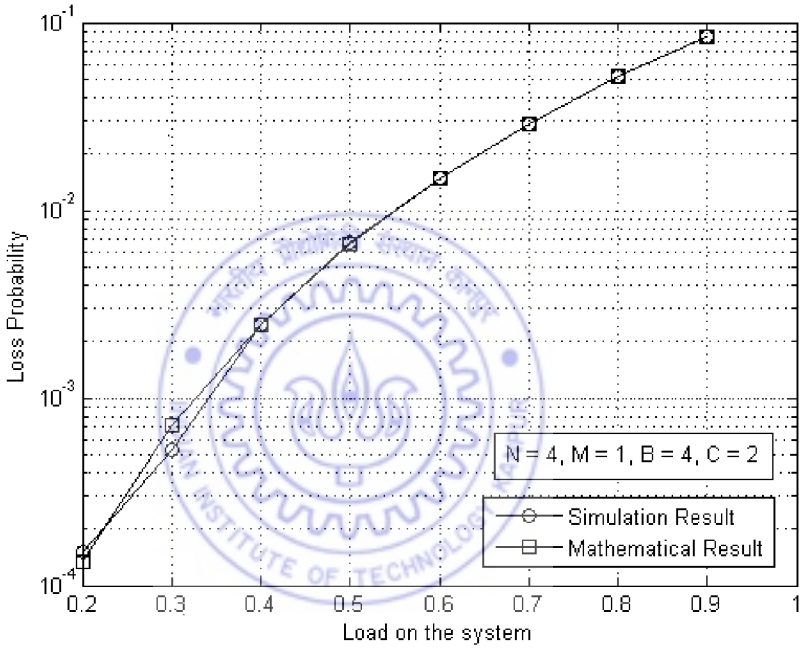


Figure 5.20: Comparative results for simulation and mathematical method.

5.6 Summary

We have presented the architecture of an optical packet switch with feedback shared buffering using WDM loop buffer modules. The application of modular structure reduces the need for a large range of wavelengths because the same set of wavelengths is used in all the buffer modules. One of the major advantages of the proposed architecture, is that the multiple loop buffer modules act together as one single fully shared

buffer while using a smaller number of wavelengths. Due to the reuse of wavelength range, the bandwidth of certain components e.g., EDFA and TWC does not restrain the total number of the buffer modules or the buffering capacity.

We have calculated the number of maximum allowed circulations in the loop buffer for correct reception of a packet. In order to focus on the performance of the switch, the analysis is done under the assumption of single node network, instead of the network consisting of several such switches. The optimal value of switch parameters, to achieve the best packet loss probability at a reasonable delay performance, has been determined. After comparing the results for several switch sizes, we found that the packet loss probability depends heavily on number of buffer modules. For smaller values of C, there will be no effect of increasing the value of M. Hence, M should be increased in accordance with C.

The simulation results are verified by comparing it with the performance of the mathematical model. This switch architecture is scalable, but the main constraint is the requirement of a large number of TWCs and other optical components. Another constraint is the number of maximum allowed circulations which decreases with increase in the switch size.

Chapter 6

AWG and EDFA based Optical Packet Switch using Feedback Shared Buffer

In this chapter, we propose an enhancement to the optical packet switch architecture (discussed in chapter 5) which uses feedback shared loop buffer modules. The main disadvantage of that architecture is very high loss in signal power which reduces the number of maximum allowed circulations by the packets in loop buffer modules. The buffering duration in the recirculating loop is limited by this circulation limit. Thus to reduce the power loss, we propose two modifications: i) either an extra optical amplifier (EDFA) is placed at the output of the loop in the buffer module, or ii) the core space switch is replaced by an AWG. The main objective of these modifications is to increase the number of maximum allowed circulations. This will effectively provide a relaxation in the circulation limit, which in turn results in the lower packet loss probability and the average delay by effectively utilizing the available buffer capacity.

6.1 Feedback Optical Packet Switch Architectures: An overview

The feedback optical packet switch architecture of chapter 5 is again shown in Figure 6.1. The core of this architecture is a nonblocking space switch of dimension $2N \times 2N$. The lower N ports (indexed 1 to N) of the core switch are used as switch inputs/outputs and the upper N ports (indexed $N+1$ to $2N$) are used for buffering of packets in the optical loop buffer modules (Figure 6.2). In this configuration, the maximum number of allowed buffer modules are $m = \lfloor N/D \rfloor$, where D is the number of inputs/outputs for each loop buffer module. The packet stored in these buffer module will keep on recirculating, till the contention is resolved. The details and working of the original switch were described in Chapter 5. We will use the word 'original' in this chapter to refer to that switch.

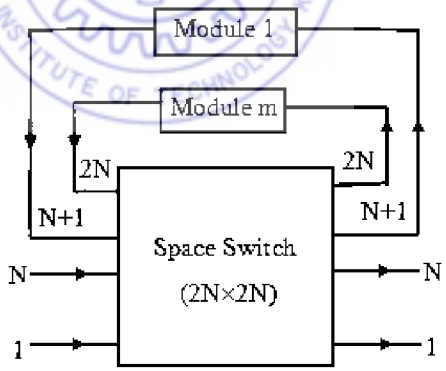


Figure 6.1: Optical packet switch architecture. Modules (1 to m) represent loop buffer modules, each with B wavelength.

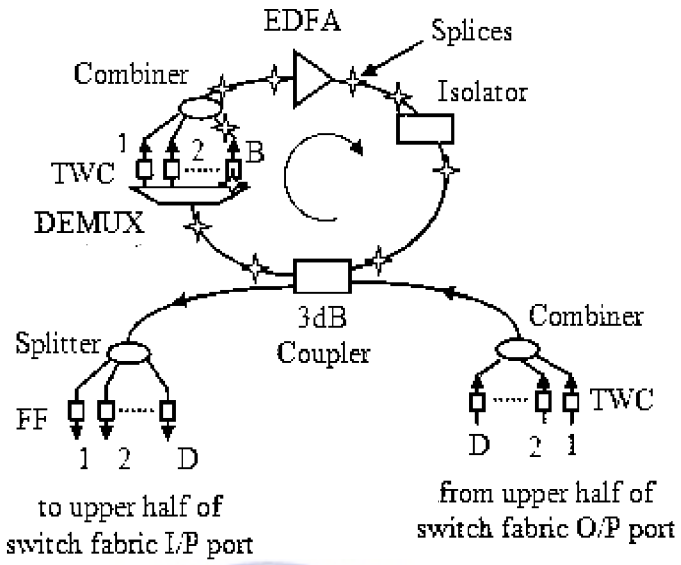


Figure 6.2: Loop Buffer Module.

6.2 Proposed Modifications in Optical Packet Switch Architectures

The number of maximum allowed circulations (C) in the recirculating loop is limited by the loss in signal power due to the presence of various optical components (Figure 6.2). The proposed modifications are intended towards increasing the value of C. The modified switch architectures are discussed below.

6.2.1 Placement of an optical amplifier (EDFA)

We place an optical amplifier (EDFA) at the output of the recirculating loop, just after the 3dB coupler (Figure 6.3). This EDFA is followed by the splitter, FF and space switch. The gain of this EDFA is chosen such that it will compensate for the loss through these three components. Effectively, it will allow the packets to circulate for some more duration as compared to the original switch, and will result in lowering

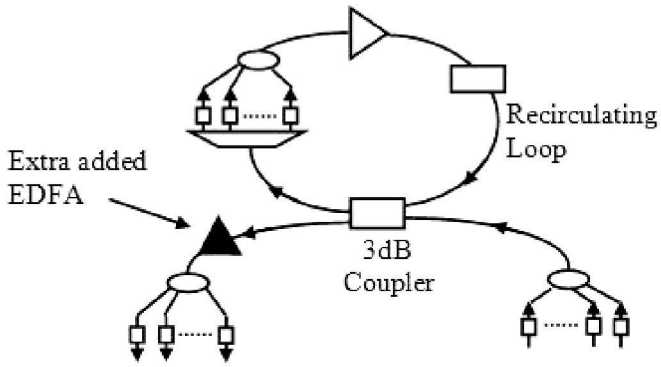


Figure 6.3: Modified Loop Buffer Module: Placement of an extra EDFA in each buffer module.

the packet loss probability. The control complexity will remain same as of the original switch. We will refer to this modification as Mod-EDFA in the following text.

6.2.2 Replacement of space switch with AWG

The core of space switch is replaced by an Arrayed Waveguide Grating (AWG) (Figure 6.4). The main advantage of the AWG is that it will avoid the need of a Splitter and the Fixed Filter at the output of the loop buffer module (Figure 6.5). The only change in working of this switch will be that, the TWC of loop will now tune the outgoing packet to a specific wavelength depending upon the input of the AWG at which the module is connected and the desired output port of the AWG. This reduces the signal power loss, and increases the number of maximum allowed circulations. We will refer to this modification as Mod-AWG in the following text.

The use of AWG necessitates the placement of TWCs at the inputs, indexed 1 to N, of the switch (Figure 6.4). The controller instructs these TWCs to change the wavelengths of the incoming packets, so that they may be automatically forwarded to the correct output because of the wavelength-dependent self-routing nature of the

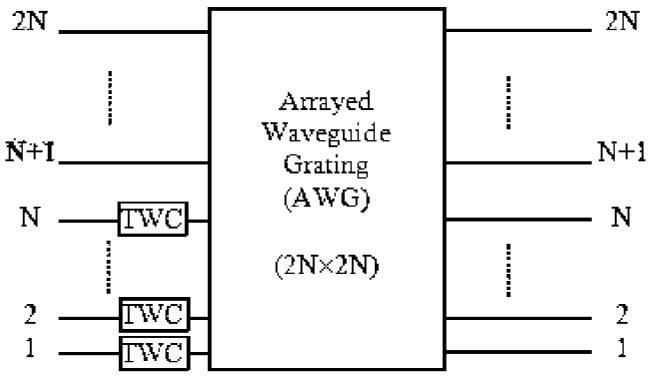


Figure 6.4: Modified switch: Replacement of core space switch with AWG.

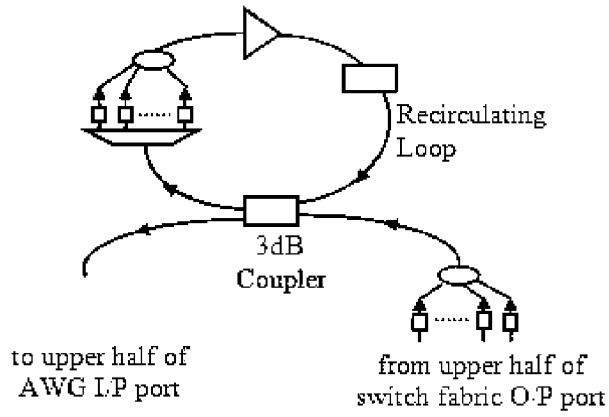


Figure 6.5: Modified Loop Buffer Module for AWG as the core of switch architecture.

AWG. If the inputs of an $N \times N$ AWG are numbered from 1 to N and its operating wavelengths range from 1 to n, then the wavelength that connects the i^{th} input to j^{th} output can be expressed as $\lambda(i,j) = \lambda_k$, where $k = [1 + (i + j - 2) mod N]$. The control complexity will be reduced due to this wavelength-dependent self-routing nature of the AWG.

6.3 Power Budget Analysis

The original switch was analyzed in terms of loss, power and noise in Chapter 5. Here, we will briefly discuss the modified expressions and also the final form of these equations. The modified switches are analyzed separately in Sections 6.3.1 and 6.3.2 for Mod-EDFA and Mod-AWG respectively. The calculation of circulation limit considering the loss, power and noise analysis is the same for both the modifications. Hence, it is discussed in Section 6.3.3.

6.3.1 Mod-EDFA

The EDFA is placed to compensate the power loss through the optical components which are following it. The gain of EDFA is denoted as G' in the following text.

6.3.1.1 Loss Analysis

The expression for Insertion loss (A_{ins}), Extraction loss (A_{ext}) and Recirculation loss (A_{re}) will still remain the same as for the original switch because the gain of this extra

added EDFA will only affect the power terms. These losses are given as,

$$A_{ins} = L_{SS}L_{TWC}L_{Com} \quad (6.3.1)$$

$$A_{re} = (A_L)^K \quad (6.3.2)$$

$$A_{ext} = L_{SP}L_{FF}L_{SS} \quad (6.3.3)$$

where $A_L = (A_1A_2)$ and

$$A_1 = L_{3dB}L_{DEMUX}L_{TWC}L_{Com}(6L_S)L_{F1} \quad (6.3.4)$$

$$A_2 = L_{ISO}(4L_S)L_{F2} \quad (6.3.5)$$

Thus, the total loss through the switch architecture is

$$A = A_{ins}A_{re}L_{3dB}A_{ext} \quad (6.3.6)$$

Various parameters and their values, used in the this analysis, are given in Table 5.1. These terms are already explained in Chapter 5, and we include them here, only to refer to them in the next section (6.3.2) dealing with Mod-AWG.

6.3.1.2 Power Analysis

We have already observed for the original switch that the inclusion of TWC noise, will not affect the system performance significantly (Figure 5.18 and 5.19). Thus we will analyze both the modified switches considering TWC as a noiseless device only.

If we follow the signal path, then the power levels of bit '1' and '0' entering at the

input of the loop of the buffer module (Figure 6.2 and 6.3) are

$$P_{in}(1) = P_{av}A_{ins}\left(\frac{2\epsilon}{1+\epsilon}\right) \tag{6.3.7}$$

and

$$P_{in}(0) = P_{av}A_{ins}\left(\frac{2}{1+\epsilon}\right) \tag{6.3.8}$$

where P_{av} is average signal power at the switch input. The signal power, after performing K circulations in the recirculating loop, will be

$$P_{out}(b) = [P_{in}(b) + K(G-1)n_{sp}h\nu B_o A_2]L_{3dB} \tag{6.3.9}$$

Here, $b = 1$ for bit '1' and 0 for bit '0'. The second term of Equation 6.3.9 is the ASE noise power added by the EDFA placed inside the loop. The extra added EDFA will also introduce ASE noise to the signal power. Thus, the final power for bit 'b' at the output of the switch is given as

$$P(b) = P_{out}(b)A_{ext}G' + (G'-1)n_{sp}h\nu B_o A_{ext} \tag{6.3.10}$$

The gain (G') is considered equal to $1/A_{ext}$ in order to cancel the lossy effect of the optical components following it i.e., $G' = 1/A_{ext}$ (Figure 6.3). Thus, the power term will become

$$P(b) = P_{out}(b) + (G'-1)n_{sp}h\nu B_o A_{ext} \tag{6.3.11}$$

The second term of the Equation 6.3.11 represents the ASE noise introduced by the extra EDFA.

6.3.1.3 Noise Analysis

Due to square law detection by the photodetector in the receiver, various noise components are generated [47]. The variance of these noise components are given as

$$\sigma_s^2 = 2qRP(b)B_e \tag{6.3.12}$$

$$\sigma_{sp-sp}^2 = R^2P_{sp}^2(K)(2B_o - B_e)\frac{B_e}{B_o^2} \tag{6.3.13}$$

$$\sigma_{sig-sp}^2 = 4R^2P(b)\frac{P_{sp}(K)B_e}{B_o} \tag{6.3.14}$$

$$\sigma_{s-sp}^2 = 2qRP_{sp}(K)B_e \quad and \tag{6.3.15}$$

$$\sigma_{th}^2 = \frac{4kTB_e}{R_L} \tag{6.3.16}$$

where,

$$P_{sp}(K) = [K(G-1)n_{sp}h\nu B_oA_2L_{3dB}G' + (G'-1)n_{sp}h\nu B_o]A_{ext} \tag{6.3.17}$$

Here σ_s^2, σ_{sp-sp}^2, σ_{sig-sp}^2, σ_{s-sp}^2 and σ_{th}^2 are variances of shot noise, ASE-ASE beat noise, sig-ASE beat noise, ASE-shot beat noise and thermal noise respectively. The term $P_{sp}(K)$ is the spontaneous noise power, and it is nearly similar to the Equation 5.4.35. The additional term is the ASE noise due to the extra added EDFA.

6.3.2 Mod-AWG

The replacement of the space switch with an AWG requires the use of TWCs (Figure 6.4). So, the loss through these TWCs need to be considered in the loss analysis. Since this modification removes the splitters and FFs placed at the output of loop in the buffer module (Figure 6.2 and 6.5), the loss analysis will also need to be changed accordingly.

6.3.2.1 Loss Analysis

The placement of AWG, will modify the expression of Insertion loss (A_{ins}) and Extraction loss (A_{ext}), while the Recirculation loss (A_{re}) will remain same. The modified expressions are given as

$$A_{ins} = L_{TWC}L_{AWG}L_{TWC}L_{Com} \quad (6.3.18)$$

$$A_{ext} = L_{AWG} \quad (6.3.19)$$

The other terms will remain same as given in section 6.3.1.1.

6.3.2.2 Power Analysis

The power analysis will be done as explained in section 6.3.1.2, but using the modified expression of A_{ins} and A_{ext}, and selecting $G' = 1$. The final output power for bit 'b' will be written as

$$P(b) = P_{out}(b)A_{ext} \quad (6.3.20)$$

6.3.2.3 Noise Analysis

The noise analysis will remain the same as done in section 6.3.1.3. Only the expression of spontaneous noise power will be changed using $G' = 1$, and is given as

$$P_{sp}(K) = K(G-1)n_{sp}h\nu B_o A_2 L_{3dB} A_{ext} \quad (6.3.21)$$

6.3.3 Calculation

The bit-error rate for both the modifications will be obtained using the same method. The total noise variance for bit 'b' is

$$\sigma^2(b) = \sigma_s^2 + \sigma_{sp-sp}^2 + \sigma_{sig-sp}^2 + \sigma_{s-sp}^2 + \sigma_{th}^2 \quad (6.3.22)$$

The bit-error rate [47] can be obtained as

$$BER = Q\left(\frac{I(1) - I(0)}{\sigma(1) - \sigma(0)}\right) \quad (6.3.23)$$

where $Q(x)$, the error function, is defined as

$$Q(z) = \frac{1}{\sqrt{2\pi}} \int_z^{\infty} exp(-z^2/2)dz \quad (6.3.24)$$

The terms $I(1) = RP(1)$ and $I(0) = RP(0)$ are photocurrents, sampled by the receiver during bit '1' and bit '0' respectively, and R is the responsivity of photodetector.

We have calculated the number of maximum allowed circulations (C) at different power levels (in mW) for both the modifications. The number of circulations C is the largest value of K (circulations count) for which, $BER \leq 10^{-9}$. The values of C are compared in Table 6.1 for $2N = 32$, $B = 4$ and $D = 4$ at $P = 1, 2, 5$ and $10mW$.

6.4 Simulation Analysis and Results

The modifications proposed in this chapter will not change the scheduling algorithm of the original switch (as described in chapter 5). Using that algorithm, the simulations are

Type of Switch	**C** **at** $P = 1mW$	**C** **at** $P = 2mW$	**C** **at** $P = 5mW$	**C** **at** $P = 10mW$
Original Switch	2	5	13	26
Mod-EDFA	27	56	140	282
Mod-AWG	3	6	16	33

Table 6.1: Maximum number of allowed circulations (C) for switch of size $2N = 32$, $B = 4$, $D = 4$ at different power levels

done and the results for '*packet loss probability*' and '*average packet delay*' are obtained for both the modifications. These results are compared with those of the original switch for the parameter values $2N = 32$, $B = D = 4$. As defined earlier, 16 of 32 ports are the actual inputs and the other 16 ports are used to connect the buffer modules.

The number of maximum allowed circulations is more for Mod-EDFA as compared to Mod-AWG (Table 6.1). In case of Mod-EDFA, there will not be any circulation limit at any power level, because the maximum capacity is still less than the number of maximum allowed circulations. For the example of $2N = 32$, the maximum buffering capacity is 16 ($= M \times B$) and $C = 27$ at $P = 1mW$. In case of Mod-AWG, since $C = 3$ at $P = 1mW$ and 6 at $2mW$, so there will be a circulation limit. Hence, the packet loss probability should be less for Mod-EDFA as compared to others. It has been observed in the simulation results that the loss probability is lower for both the modifications as compared to the original switch (Figure 6.6 and 6.7). Also, if we only compare the two proposed modifications, the Mod-EDFA is much better than Mod-AWG.

The average delay performances for the modified switch of size $2N = 32$ are shown in Figure 6.8 and 6.9. We observe that the delay increment for the two cases of modifications is not very significant, and is overshadowed by the advantages obtained in terms of loss probability.

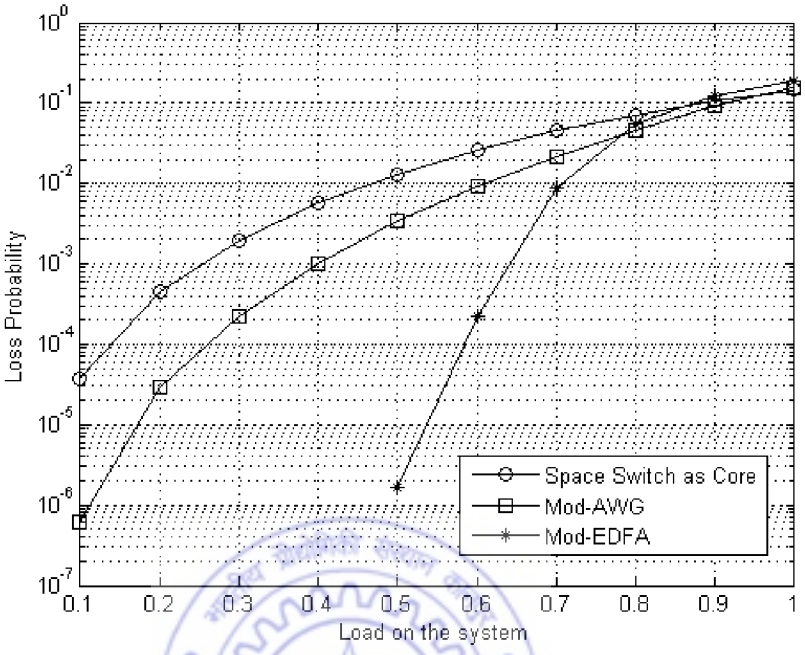


Figure 6.6: Loss probability for $2N = 32,\ D = 4,\ B = 4,\ M = N/D$ and $P = 1mW$.

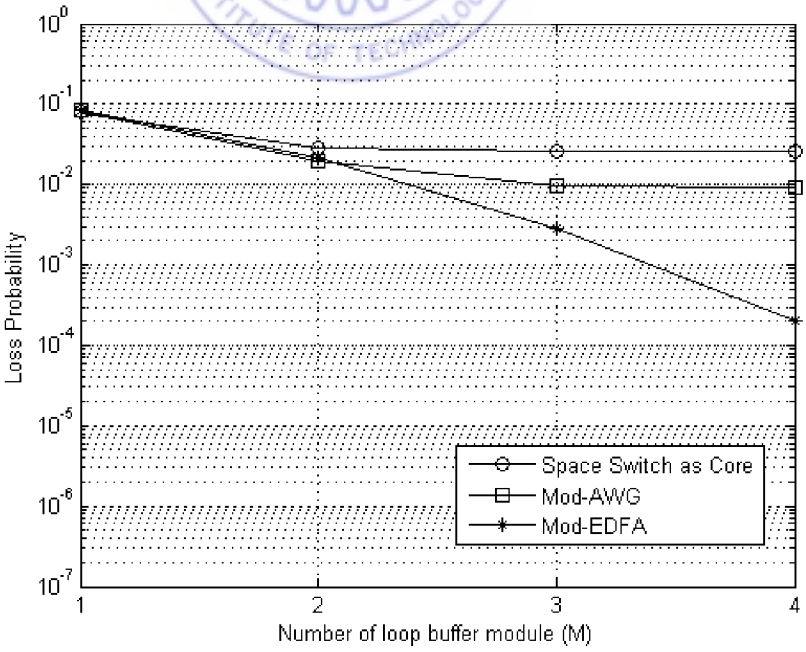


Figure 6.7: Loss probability for $2N = 32,\ D = 4,\ B = 4$, Load $= 0.6$ and $P = 1mW$.

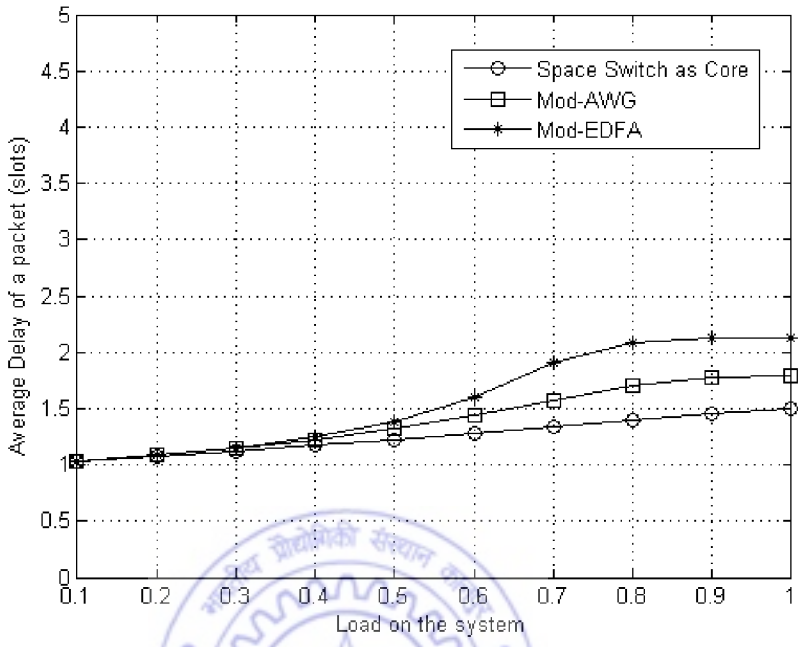


Figure 6.8: Average delay for $2N = 32,\ D = 4,\ B = 4,\ M = N/D$ and $P = 1mW$.

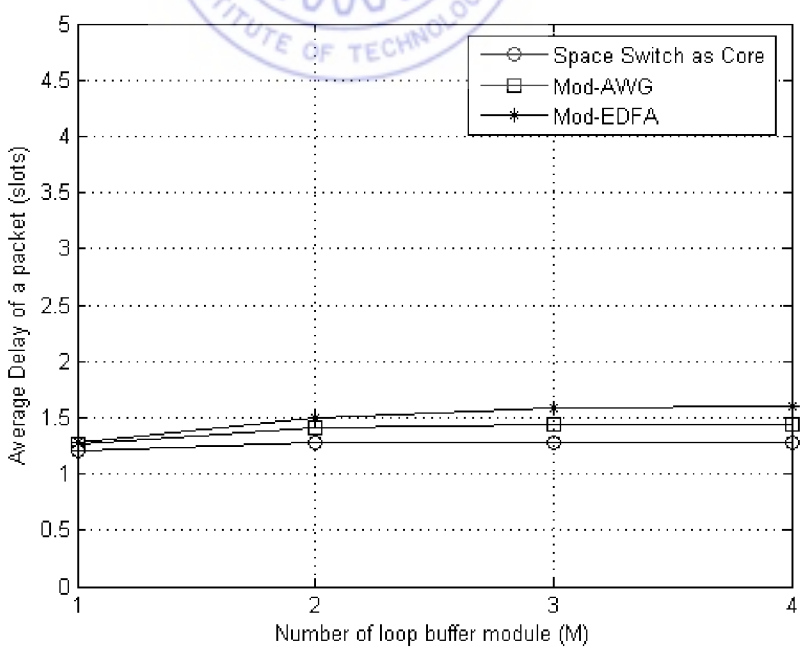


Figure 6.9: Average delay for $2N = 32,\ D = 4,\ B = 4$, Load $= 0.6$ and $P = 1mW$.

6.5 Summary

We have presented the modified architectures of an optical packet switch with shared feedback-buffering using WDM loop buffer modules. The modular structure reduces the need for a large range of wavelengths because the same set of wavelengths is used in all the buffer modules.

The objective of the switch improvements described in this chapter was to increase the number of maximum allowed circulations of the packet in the loop buffer module. We have calculated it for both the modifications. These numbers imply that the circulation limit is relaxed for Mod-AWG while there is no circulation limit for Mod-EDFA. The results for packet loss probability and average delay are compared, and they indicate that the proposed modifications give enhanced performance.

In order to focus on the performance of the switch, the analysis is done under the assumption of a single node network instead of the network consisting of several such switches. We can also apply these switches in large networks, but the related issues need further investigations.

Chapter 7

Wavelength routed shared buffer based feed-forward architectures for optical packet switching

In this chapter, we are proposing three architectures[1] for optical packet switching based on wavelength routed feed-forward shared buffer modules [60]. These architectures are developed by selecting three different combinations of space switches and Arrayed Waveguide Gratings (AWG). The buffer modules are constructed using recirculating type fiber delay lines incorporating various optical components [55]. These recirculating loop buffers are designed for fixed length packets. One of these architectures has also been analyzed in terms of power loss and noise power due to the presence of various optical components in the loop buffer module. The performance is predicted on the basis of operational insights. Further, it has been verified by getting the results using simulations. For convenience, the notations A1, A2 and A3 will be used for the three architectures being proposed in this chapter.

[1] "Wavelength routed shared buffer based feed-forward architectures for optical packet switching," *Proc. IEEE INDICON Conf.*, Sep' 2006, New Delhi.

7.1 Description of the Architecture A1

The basic building block of all the three architectures has a similar structure, and consists of three sections:

1. Scheduling section,
2. Combined section (Path section) for routing the packet through either 'M' direct paths or 'm' buffer modules, and
3. Switching section.

This section will discuss only the architecture A1 while the other two architectures (i.e., A2 and A3) will be discussed in the later sections. The switch architecture A1 and its buffer module are shown in Figure 7.1 and 7.2 respectively. The scheduling and switching section of A1 are constructed using space switches. The size of these sections will be $N \times K$ and $K \times N$ respectively, while the overall size of the switch architecture is $N \times N$. The parameter K is defined as $K = M + m \times D$, where M is the number of direct path with no delay, m is the number of loop buffer modules used in the feed-forward manner, and D is the number of inputs/outputs ports assigned to each buffer module. The capacity of each buffer module is considered equal to B ($\geq D$) i.e., it can store up to B number of packets at different wavelengths. The range of these wavelengths will be different from the incoming wavelengths. Also, the same range of buffer wavelengths can be reused in all the buffer modules, because the packets present in different buffer modules are independent and do not interfere.

Each buffer module consists of D tunable wavelength converters (TWCs), a recirculating loop and one wavelength demultiplexer (DEMUX) (Figure 7.2). The packets

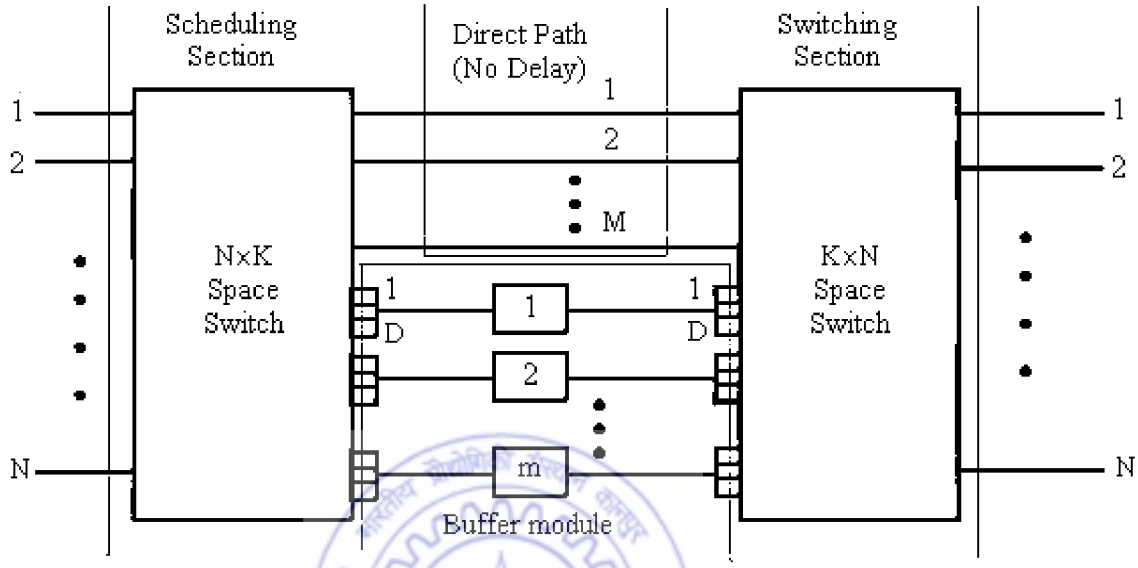


Figure 7.1: Switch Architecture - A1

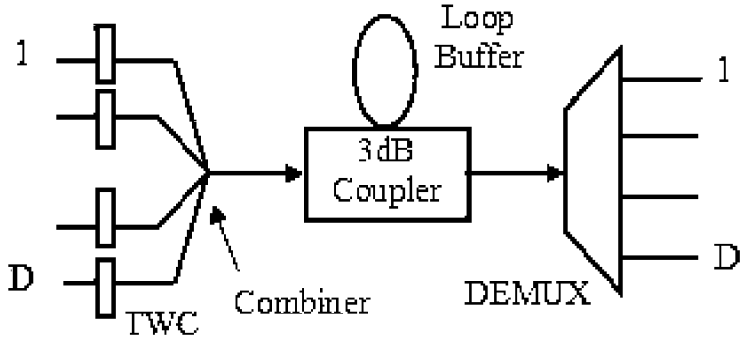


Figure 7.2: Buffer module for A1

from all these D inputs use WDM to share the recirculating loop buffer. The wavelength range of DEMUX, is chosen to be different from the range of buffer wavelengths to prevent direct transfer of packets bypassing the recirculating loop. This loop buffer module is nearly similar to the feedback switch (Figure 5.3). The only difference is that the DEMUX is used at the module output of this chapter, in place of Splitter and Fixed Filters. The recirculating loop consists of a 3dB Coupler, DEMUX, TWCs, Combiner, EDFA, Isolator and Band Pass Filter (BPF) (Figure 7.3). The EDFA is placed inside the loop to compensate for the power loss in the loop buffer during circulation, and the BPF is used to band-limit the ASE noise. More details about functioning of this buffer module were provided in Chapter 5.

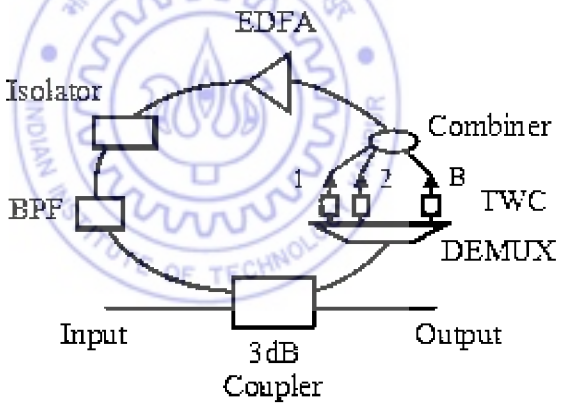


Figure 7.3: Architecture of recirculating loop

7.2 Scheduling Algorithm

The buffering technique of the proposed architectures utilizes the loop buffer module in feed-forward configuration. If any packet is directed towards the buffer modules due to contention, then it will keep on circulating inside the loop till the contention is resolved. The term "Feed-Forward" means that once the packet arrive at the input, due

to contention, it will be passed to a loop buffer which is not connected to the input of that input stage. Instead, the loop buffer is connected to the next stage. This indicates that the packet moves only in the forward direction. While in the feedback case, the loop buffer is connected to the input section of same stage, which results in the packets entering at the input stage many times.

The scanning of input ports for the arriving packets is done sequentially during the simulation. The arriving packets may contend for an output in two ways: i) contention among themselves or ii) contention with already stored packets in the buffer. During contention of any type, priority will be given to the already stored packets in the buffer modules and then if possible, the rest of the contending packets will be buffered. FCFS scheme is considered for routing, so that no packet is delayed indefinitely. Direct path will only be used when no packet in any of the buffer modules is destined for that output port.

The number of buffered packets (x_j) for the output j, should never be greater than the maximum buffering capacity $m \times B$ i.e., $x_j \leq mB$. Also, the total amount of buffered packets, cannot be larger than $m \times B$ i.e., $\sum x_j \leq mB$. The storage principle for a packet in the buffer module will remain same as given in Chapter 5. Since a DEMUX is used here, a change occurs only during the readout of packet. Hence for reading out a packet, the corresponding TWC inside that loop is now tuned to the free wavelength at the DEMUX output port, and then the packet is directed towards switching section through this DEMUX. Finally, these scheduled packets on reaching the switching section will be switched to the destined output port through the space switch fabric.

7.2.1 Performance Evaluation

We have simulated the architecture A1 to evaluate the performance in terms of packet loss probability and average delay. The arriving traffic is considered to be uniformly distributed and random in nature. We have done the simulations by applying a heuristic approach for the selection of various combinations of B, M and m for a particular switch of $N = 16$ with $D = 4$ under different loading conditions. Several combinations of M and m are used for the values of B as 4, 8 and 12. Only those results are shown in Figure 7.4, which provide the packet loss probability up to an acceptable level. We have chosen three best combinations, one for each case of $B = 4,\ 8$ and 12. These are termed as $C1$, $C2$ and $C3$ respectively, and can be written as

$$C1 : B = 4,\ M = 8,\ m = 6,\ K = 32$$

$$C2 : B = 8,\ M = 4,\ m = 4,\ K = 20$$

$$C3 : B = 12,\ M = 4,\ m = 4,\ K = 20$$

We found that the value of K is different and greater than N for these three combinations. Since, the space switch can be asymmetrical in size (i.e., $K \geq N$ for switch of size $N \times K$ and $K \times N$), so all the three combination are possible, but we have to select the suitable combination.

7.2.1.1 *Combination selection using simulation results*

The average delay for a packet using the switch of size $N = 16,\ D = 4$ and combinations $C1$, $C2$ and $C3$ is shown in Figure 7.5. We can observe that under lower loading conditions, the delay performance is same for all the three combinations while at higher loads, the average delay increases significantly for $C3$. Thus we obtain lower loss probability for $C3$ as compared to $C1$ and $C2$ (Figure 7.4) but at the cost of increased delay.

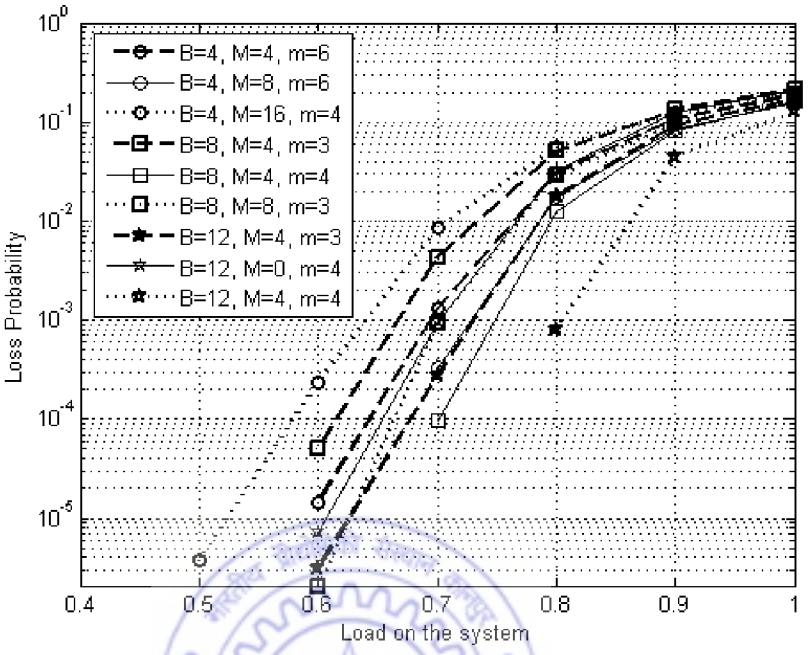


Figure 7.4: Loss probability for $N = 16$ with various combination of B, M and m

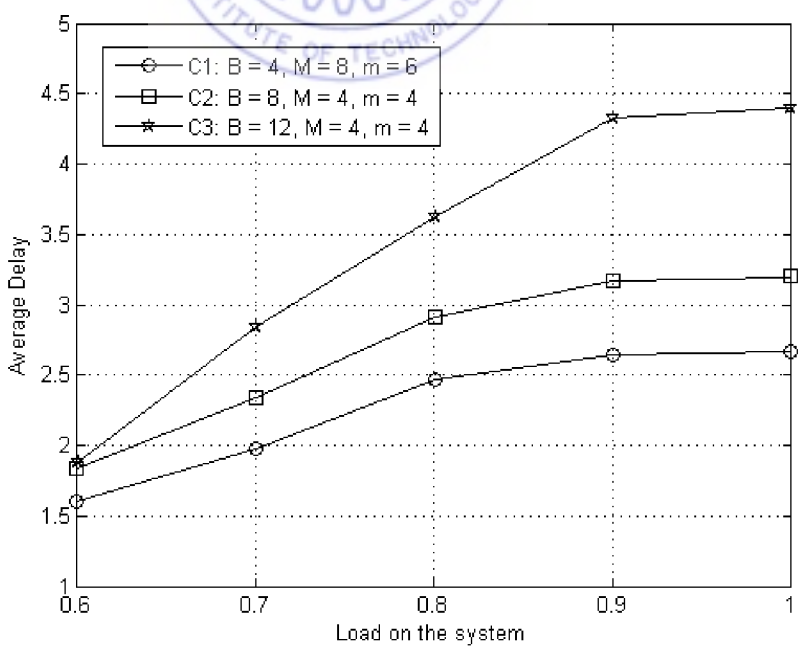


Figure 7.5: Comparison of Average Delay for $C1,\ C2,\ C3$ at $D = 4$ and $N = 16$

Thus, we will also compare the size/number of the optical components used for each of the three combinations, to find out the suitable choice among the three combinations.

7.2.1.2 *Combination selection in terms of component complexity*

The major components and their size/quantity used in A1 for the above three combinations are compared in Table 7.1. The size of scheduling and switching stage are asymmetrical for each case but larger for $C1$, and the same for $C2$ and $C3$. The number of TWCs ($= D \times m + B \times m$) are same for $C1$ and $C2$, and higher for $C3$. The number of DEMUX is highest for $C1$ while it is same for $C2$ and $C3$. On the other hand, size of DEMUX used inside the recirculating loop will be smallest for $C1$ (i.e., 1×4) while largest for $C3$ (i.e., 1×12), and so is the insertion loss. Hence, there will be a trade-off between the number and size of DEMUX, and this indicates that $C2$ will be the better choice in terms of DEMUX usage.

Another important parameter is the gain of the EDFA placed inside the recirculating loop. Since in the case of $C3$, the maximum number of wavelength channels are used for buffering ($B = 12$), thus the EDFA used in this case will be of highest gain to compensate the loss of 1×12 DEMUX (Table 7.1). Similarly, the gain of EDFA used in $C1$ will be lowest as the value of B is 4. The EDFAs will also produce amplified spontaneous emission (ASE) noise which increases alongwith the gain of EDFA. Since ASE noise is a degrading factor so, it should be as low as possible and so is the gain. Thus, $C2$ will be the better choice in term of using EDFA because its gain lies between the gain of EDFAs used for $C1$ and $C3$. Hence, the suitable choice among the three combinations of parametric values is $C2$ i.e., $B = 8,\ M = 4,\ m = 4$ for $D = 4$ and $N = 16$.

Combination of values	**Size of Scheduling section** $N \times K$	**Size of switching section** $K \times N$	**Total number of TWC**	**Total number of DEMUX (Inside+Outside) of loop**	**Gain of EDFA**
$C1$	16×32	32×16	48	$6(1 \times 4) + 6(1 \times 4) = 12$	Lowest
$C2$	16×20	20×16	48	$4(1 \times 8) + 4(1 \times 4) = 8$	Medium
$C3$	16×20	20×16	64	$4(1 \times 12) + 4(1 \times 4) = 8$	Highest

Table 7.1: Complexity analysis of major component used in architecture A1 for three efficient combinations at $D = 4$ and $N = 16$

We can generalize the combination C2 as $B = 2D$, $M = N/4$ and $m = N/D$ for larger values of N and D. The effect of increasing switch size alongwith the other parameters is examined, using this generalized form of combination $C2$. Figure 7.6 shows the packet loss probability with increasing load for various sizes of switch. Figure 7.7 shows the packet loss probability with increasing switch size for various loading conditions. The results show that the loss probability increases with the increase in load for a particular switch size. We can also observe that the loss probability decreases with increase in switch size at a given load. This indicates that the extent to which contention occurs, reduces with increase in switch size. Since the amount of buffering is proportional to switch size, the loss probability reduces as the switch size increases. The explanation and the proof of this statement is well described in section 5.3.2.

The results for average delay are shown in Figure 7.8. It indicates that the delay is more at higher load and it is obvious because of the presence of more number of packets in the system at any instant of time. But there is not much effect of increasing the switch size. This could be because of the increment in the available buffer space and also the amount of traffic passing through switch, since both grow proportionally with the switch size.

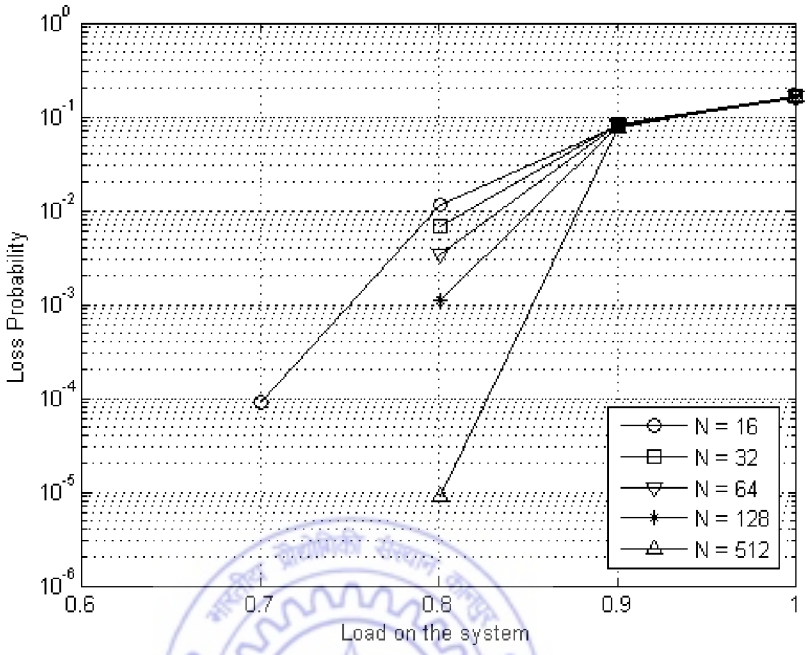


Figure 7.6: Loss probability for various switch size using $C2$ at $D = 4$

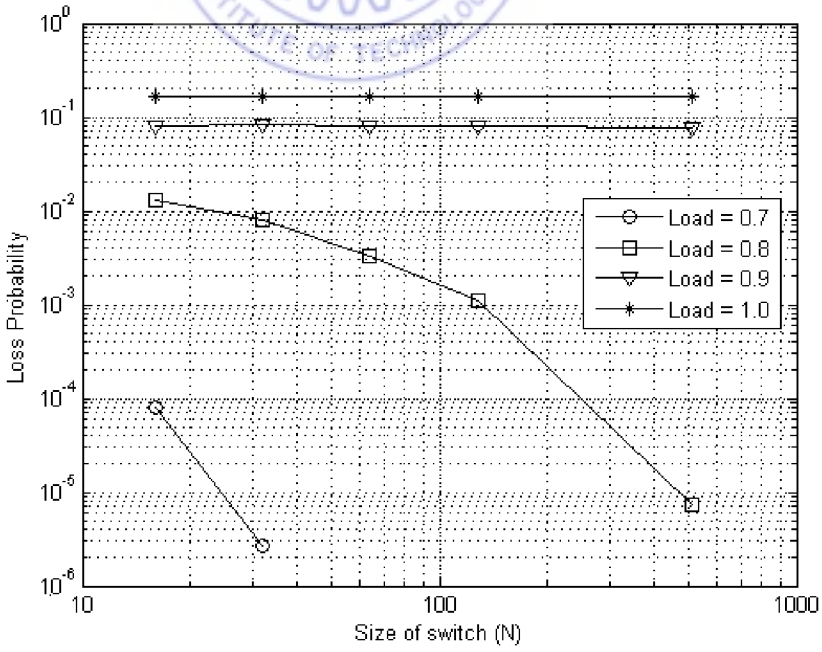


Figure 7.7: Loss probability under various load on system using $C2$ at $D = 4$

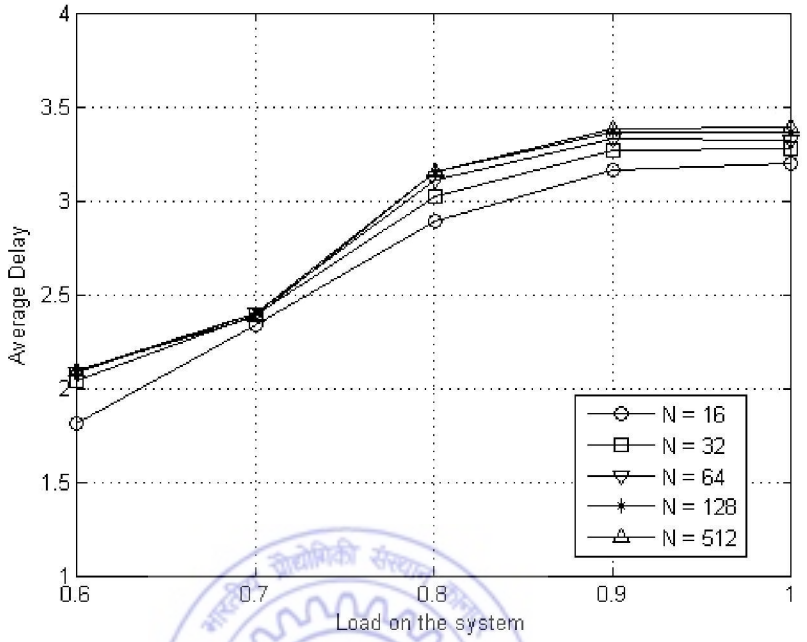


Figure 7.8: Average Delay for various switch size using $C2$ at $D = 4$

7.3 Power Budget Analysis for Architecture A1

The presence of various optical components in the loop buffer memory module causes signal power loss and addition of noise power. This will restrict the storage time (circulation count) in the loop buffer because of the degradation in packet quality during each circulation. Thus, we are required to calculate the number of maximum allowed circulations (C) for a packet before its correct reception. In other words, the packets cannot be retrieved after $(C + 1)^{th}$ revolution because the value of BER would have reached beyond the acceptable level.

The proposed switch is analyzed in terms of loss, power and noise by using the model shown in Figure 7.2 and 7.3. This analysis is done for the architecture A1 (Figure 7.1), where the size of both the section of A1 are considered as $N \times N$ (i.e., symmetrical

switch). Value and nomenclature of various parameters used in the following analysis, are reported in Table 5.1.

7.3.1 Loss Analysis

The loss analysis has been divided into three parts according to the three sections of A1 (Figure 7.1). The input (scheduling) and output (switching) sections consist of a space switch fabric, so the loss through them is defined as

$$L_{in} = L_{SS} \tag{7.3.1}$$

and

$$L_{out} = L_{SS} \tag{7.3.2}$$

Loss through the buffer module for one circulation is obtained in terms of each component loss.

$$L_{BM}(1) = L_{TWC}L_{Com}A_{LB}L_{3dB}L_{DEMUX} \tag{7.3.3}$$

where A_{LB} is the loss through the recirculating loop which consists of 8 splices [55], and is defined as

$$A_{LB} = L_{3dB}L_{DEMUX}L_{TWC}L_{Com}L_{ISO}L_{BPF}8L_SL_F \tag{7.3.4}$$

The loss of the buffer module after 'J' circulations will be,

$$L_{BM}(J) = L_{TWC}L_{Com}(A_{LB})^J L_{3dB}L_{DEMUX} \tag{7.3.5}$$

Thus the total loss through the switch architecture after J circulations,

$$L = L_{in} L_{BM}(J) L_{out} \tag{7.3.6}$$

7.3.2 Power Analysis

In this analysis, we have considered only a noiseless TWC, as we have seen in the earlier chapters that a noisy TWC does not produce a significant effect. The input power is defined as $P_{in}(b)$ where $b = 1$ for bit '1', and 0 for bit '0'. Thus the signal power after one circulation, just before the 3dB coupler, is given by

$$P_1(b) = P_{in}(b) A_1 A_{LB} G + (G-1) n_{sp} h\nu B_o A_2 \tag{7.3.7}$$

where

$$A_1 = L_{in} L_{TWC} L_{Com} \tag{7.3.8}$$

$$A_2 = L_{ISO} L_{BPF} 3 L_S L_F \tag{7.3.9}$$

In the Equation 7.3.7, first term represents the signal power, and the second term is ASE noise power added due to the EDFA [47]. Here, A_1 is the loss from switch input up to the input of 3dB coupler, and A_2 is the loss in the last portion of loop i.e., after EDFA up to the 3dB coupler input (Figure 7.3). Thus the power of bit 'b' after J circulations,

$$P_J(b) = P_{in}(b) A_1 (A_{LB})^J G^J + (G-1) n_{sp} h\nu B_o A_2 F \tag{7.3.10}$$

where

$$F = \begin{cases} \frac{1-(A_{LB}G)^J}{1-A_{LB}G}, & A_{LB}G < 1 \\ J, & A_{LB}G = 1 \end{cases} \tag{7.3.11}$$

For SNR maximization, product of gain and loop loss must be equal to unity ($A_{LB}G = 1$) [45], thus

$$P_J(b) = P_{in}(b)A_1 + (G-1)n_{sp}h\nu B_o A_2 J \tag{7.3.12}$$

Hence the power for bit 'b' at the output of the switch, is given as,

$$P(b) = P_J(b)L_{3dB}L_{DEMUX}L_{out} \tag{7.3.13}$$

7.3.3 Noise Analysis and Calculation

The noise analysis is similar to the one explained in Section 5.4.1.3 for feedback switch architecture. The procedure for calculating the gain and length of EDFA is also same as explained in Section 5.4.1.4. Depending upon those observations, the number of maximum allowed circulations (C) is obtained (Table 7.2) at different power levels (mW) with various sizes of switch (N) and number of buffer wavelength (B). The value of C is the largest value of J for which $BER \leq 10^{-9}$.

This circulation limit will also affect the maximum buffering capacity for any particular output, as given in the scheduling algorithm section. Hence, the new condition will become as $x_j \leq min(mB, C)$. The second condition of total buffering capacity will still remain same i.e., $\sum x_j \leq mB$.

N	**B**	**C at 1mW**	**C at 2mW**	**C at 4mW**	**C at 6mW**	**C at 8mW**	**C at 10mW**
16		14	28	56	84	113	141
32	4	11	22	44	67	89	112
64		8	17	35	53	71	89
16		4	9	18	27	36	45
32	8	3	7	14	21	28	35
64		2	5	11	17	22	28
16		1	2	5	8	11	14
32	12	1	2	4	6	9	11
64		0	1	3	5	7	9

Table 7.2: Number of maximum allowed circulations (C) for various sizes of switch (N) and buffer wavelength (B) at different power levels (P) considering $D = 4$.

7.3.4 Simulation Results

The simulations are done using the scheduling algorithm and the results for '*packet loss probability*' and '*average delay*' are obtained under various loading conditions. To keep the switch size equal to $N \times N$, such values of m and B are chosen which will provide minimum loss probability. For $N = 16$ and $D = 4$ at $P = 2mW$, the loss probability is minimum (8×10^{-5}) for $m = 3$ and $B = 8$ (Figure 7.9) whereas at $P = 8mW$, minimum (2×10^{-5}) is obtained for $m = 3$ and $B = 12$. The later obtained loss probability is 4 times lower than the earlier one but at the power level 4 times higher. Thus, this advantage of lower loss probability will be overshadowed by the performance degradation due to nonlinear effects in the fiber caused by such a higher power level. The average delay is same at all power levels for $B = 4$ and 8 but, it increases with power for $B = 12$ (Figure 7.10). Also, there is a sudden increase in the average delay for $m > 3$. So, we have to consider the case of $m = 3$ as the optimal choice for 16×16 switch, and will again analyze the switch to optimize the value of B for $N = 16$ and $D = 4$ at $m = 3$.

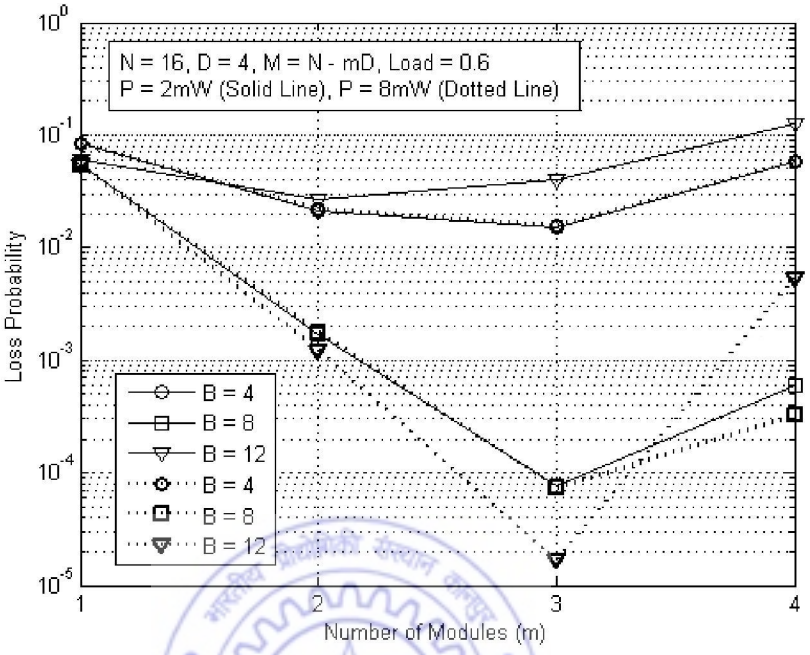


Figure 7.9: Optimization of B and m for $N = 16$ in terms of loss probability.

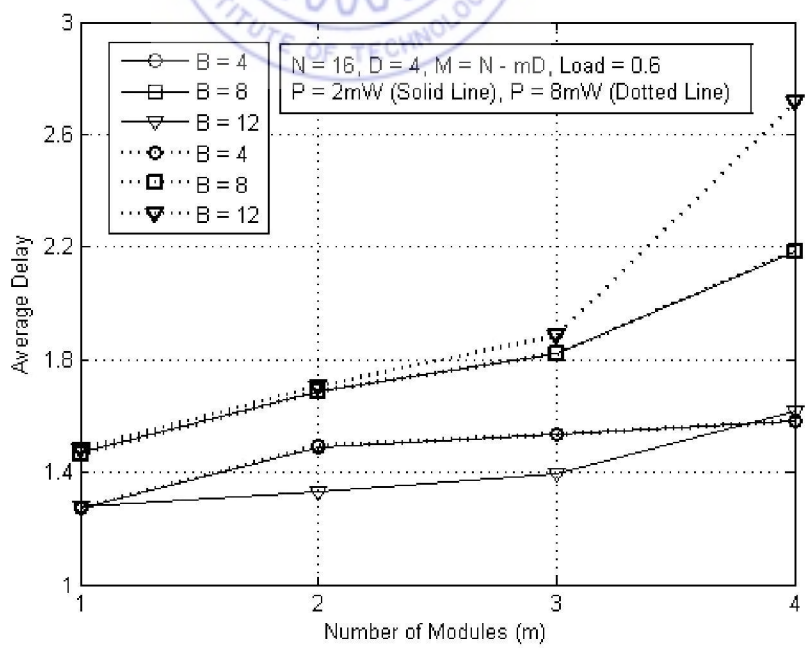


Figure 7.10: Optimization of B and m for $N = 16$ in terms of average delay (slot count).

We observe in Figure 7.11 that as the signal power increases, the probability of packet loss decreases due to the increment in C with power. The switch parameters are considered as $N = 16,\ M = 4,\ m = 3$ and $D = 4$. The maximum buffering capacity $(m \times B)$ for $B = 8$ is 24 while for $B = 12$, that will be 36. At lower power levels and under lower loading conditions, $B = 8$ gives better results as compared to $B = 12$ (Figure 7.11) because of the larger number of maximum allowed circulations for $B = 8$. But, at higher powers and under lower loading conditions, $B = 12$ gives better results as compared to $B = 8$. The reason is that the number of maximum allowed circulations in case of $B = 12$ is as good in number as achieved with $B = 8$ at lower power levels (Table 7.2). Also at higher powers, the larger number of maximum allowed circulations for $B = 8$ does not give any advantage because the maximum circulations count is limited by the available buffer capacity and not by the circulation limit. Under higher loading, the loss probability is very large for both cases.

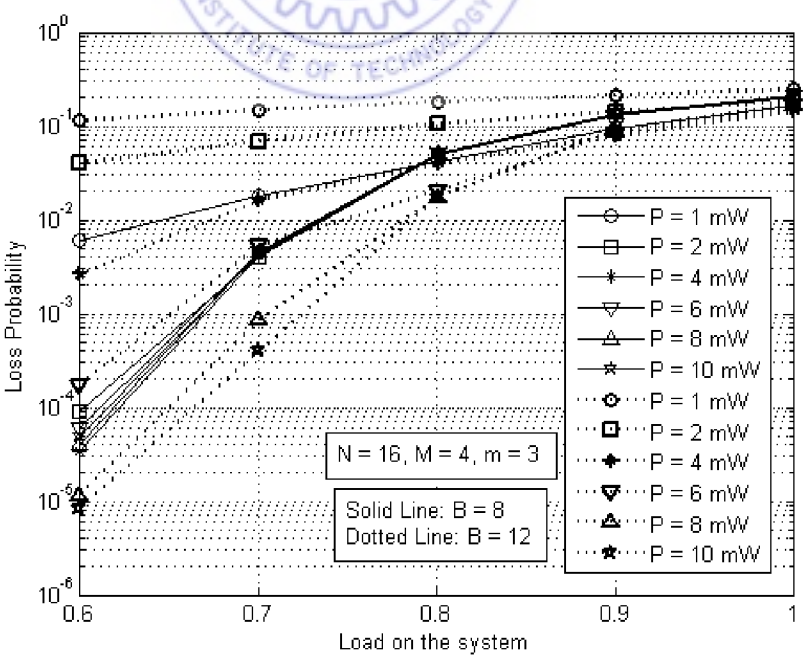


Figure 7.11: Probability of packet loss for various power levels at $D = 4$.

The average delay for $B = 8$ is nearly equal at all power levels under moderate loading conditions (Figure 7.12). The average delay for $B = 12$ increases with higher power levels due to more utilization of buffering capacity while at lower power levels, the average delay is very small and nearly constant under various loading conditions.

On the basis of above results, one may deduce that $B = 12$ should be favored over $B = 8$ because it provides better loss probability. But the main disadvantage of $B = 12$ is that the recirculating loop for this case will use larger size of DEMUX/Combiner and more number of TWCs. Also, the EDFA used in this case needs to have a higher gain. Another important issue is that, although the $B = 12$ provides better results at higher power levels (Figure 7.11), but working at such a high power level will induce the nonlinear effects into the signal. Hence, the loop buffer of capacity $B = 8$, will be a better choice. Thus the optimal choice for $N = 16$ is $D = 4,\ B = 8,\ m = 3\ \&\ M = 4$.

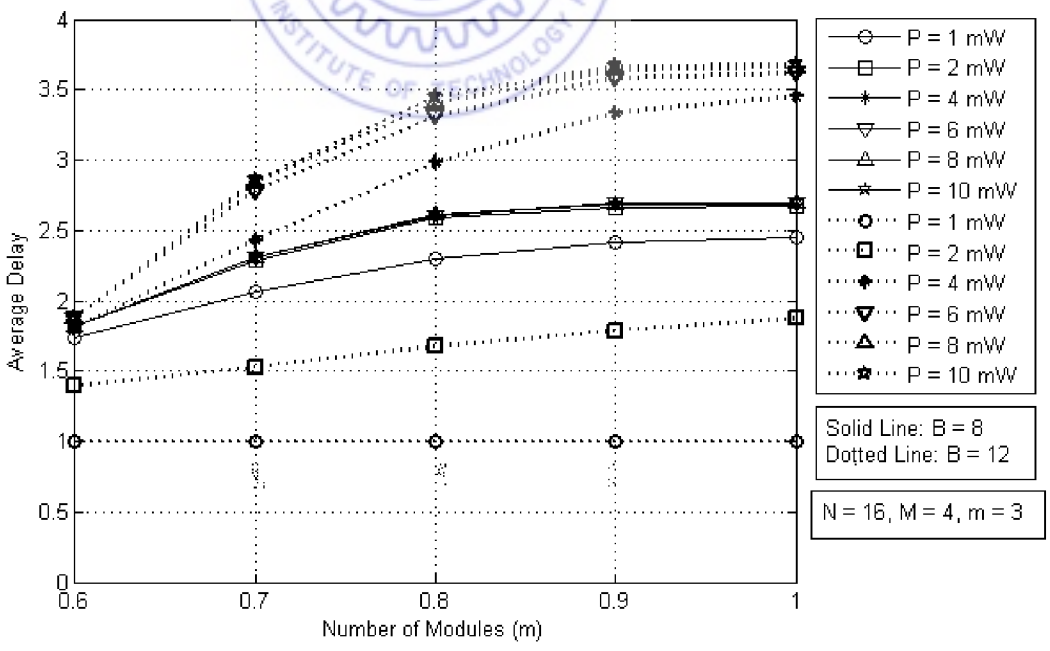


Figure 7.12: Average delay (slot count) for various power levels at $D = 4$.

7.4 Description of the Architectures A2 and A3

The architectures A2 and A3 are shown in Figure 7.13 and 7.14 respectively. Both of these architectures use same buffer module as shown in Figure 7.15. In the architecture A2, the scheduling stage is made of a space switch, and its size is same as of A1 (i.e., $N \times K$) while the switching section is made of an AWG of size $N \times N$. In the architecture A3, both of the scheduling and switching stages are made by AWGs of size $N \times K$ and $N \times N$ respectively. The architecture of the loop buffer module for A2 and A3 (Figure 7.15) will remain nearly the same as the one used in A1 (Figure 7.2). The working of switches A2 and A3, and the corresponding buffer modules will also remain same as of A1. The only difference is that the DEMUX at the output of buffer module of A1 will be replaced by a BPF for A2 and A3. The wavelength range of this BPF is chosen to be different from the range of buffer wavelengths, to prevent the direct transfer of input packets bypassing the recirculating loop.

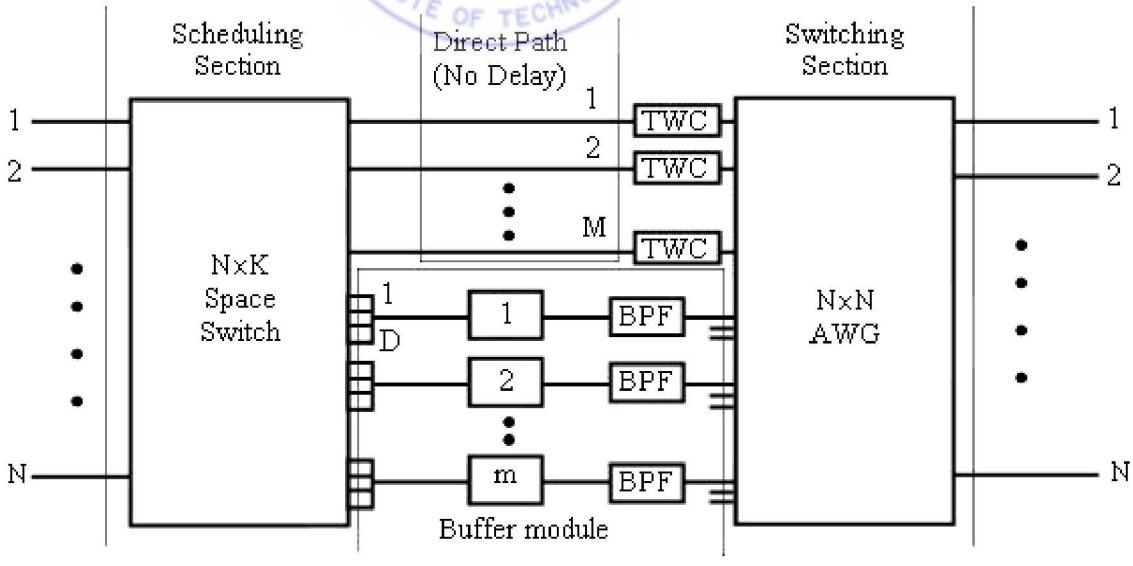


Figure 7.13: Switch Architecture - A2

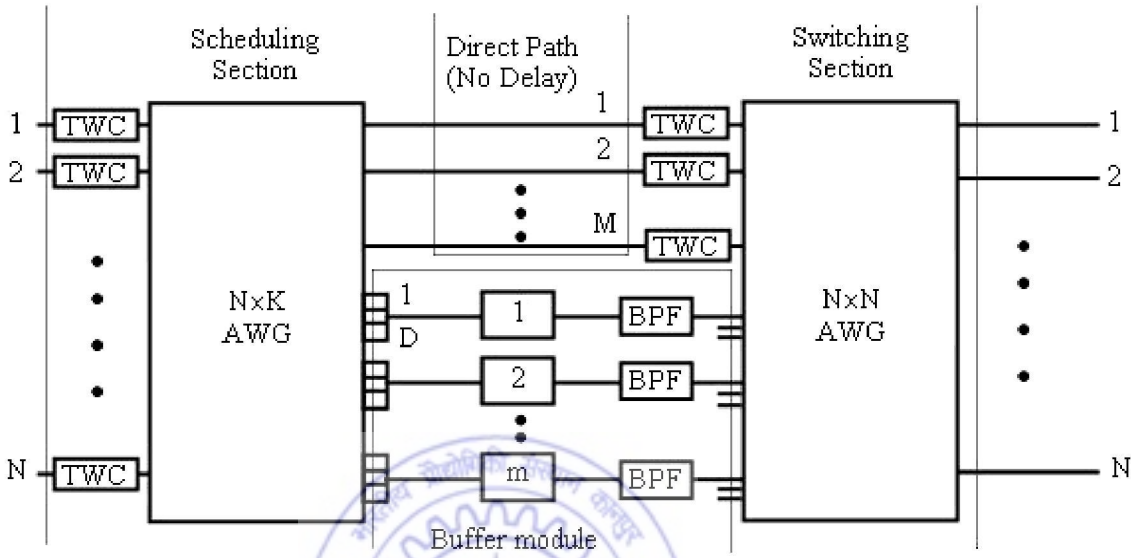


Figure 7.14: Switch Architecture - A3

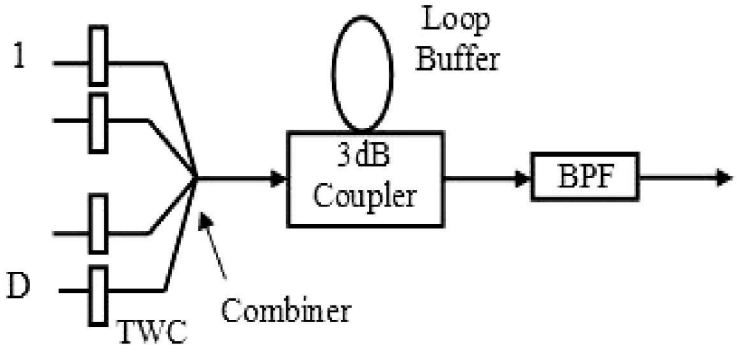


Figure 7.15: Buffer module for A2 and A3

The buffer module for A2 and A3 uses $(B + N)$ wavelengths. Here, N is the number of wavelengths used for reading out the packets from the loop buffer. Due to the wavelength dependent self-routing nature of AWG, the extra TWCs are introduced at the input of AWG. These TWCs are placed at every input of scheduling stage in A3, and in the direct path of A2 and A3. These TWCs are used to tune the incoming signal at the appropriate wavelength depending upon its destination.

7.5 Comparison among three architectures

The asymmetric space switch of size $N \times K$ (where $K \geq N$) has been demonstrated and is being used in various studies of switch architecture [28], while the asymmetric AWG have not been used in any study so far. Thus the availability of asymmetric AWG is assumed in the architecture A2 and A3, as they may become practically feasible in near future. But, in such circumstances where $K > N$ for the current use, we can use the AWG of size $K \times K$ and leave $K - N$ inputs free, in order to analyze the behavior of the switch architecture.

7.5.1 Link Loss Analysis

The maximum physical loss attained by any packet while passing through the architectures A1, A2 and A3 are obtained by adding the loss (in dB) through each component. The maximum loss for these architectures are

$$L_{A1} = L_{SS} + L_{TWC} + L_{Com} + L_{LB} + L_{3dB} + L_{DEMUX} + L_{SS} \quad (7.5.14)$$

$$L_{A2} = L_{SS} + L_{TWC} + L_{Com} + L_{LB} + L_{3dB} + L_{BPF} + L_{AWG} \quad (7.5.15)$$

$$L_{A3} = L_{TWC} + L_{AWG} + L_{TWC} + L_{Com} + L_{LB} + L_{3dB} + L_{BPF} + L_{AWG} \quad (7.5.16)$$

Here, L_{LB} is loss through the recirculating loop and is defined as

$$L_{LB} = L_{3dB} + L_{DEMUX} + L_{TWC} + L_{Com} + L_{ISO} + L_{BPF} \quad (7.5.17)$$

The path loss for any packet passing through the switch and the loop buffer module is calculated for all the three architectures using the combination $C2$ at $N = 16$ and $D = 4$. These losses are

$L_{A1} = 36.45dB$,

$L_{A2} = 35.45dB$, and

$L_{A3} = 36.95dB$.

These values are obtained by using the values of parameters, given in Table 5.1. In the above calculations, we have considered only single revolution for a packet in the recirculating loop i.e., if any packet performs more number of circulations then its loss will be more. These results indicate that physical loss remains nearly the same for a packet passing through any of the three architectures. Thus the selection of the suitable architecture depends on the controlling ability of the system as well as on the system requirements.

7.5.2 Control Complexity

There will not be any difference in the performance of all the architectures in terms of packet loss probability and average delay, because the same scheduling algorithm will be used for each case. But the implementations of these architectures require a specific set of components for their optimal operation.

The architecture A1 consists of space switch fabric at both stages i.e., at scheduling as well as switching stage, hence their control complexity is high. The architecture A2

uses AWG at switching stage while A3 uses AWG at both ends in place of space switch fabrics. There is no requirement of control of AWG due to its wavelength-specific self-routing nature. But this advantage will be countered by the presence of TWC at input ports of AWG because these TWCs also require controlling.

7.6 Summary

In this chapter we have presented three architectures having different types of scheduling and switching sections. We have compared the three architectures in terms of link loss and EDFA gain. We have also optimized the buffer parameters for better loss probability and average delay. It was found that the final three combinations of parameters are comparable among each other, and can be used accordingly.

The architecture (A1) is analyzed mathematically and found that the effect of noise imposes a limitation on the number of maximum allowed circulations for a packet in the loop buffer. Also by making an optimal choice of number of buffer modules and buffering capacity, one can obtain a better loss probability at a reasonable delay for various sizes of the switch. The optimal values for switch of size $N = 16$ are $B = 8$, $m = 3$ and $M = 4$ in case of symmetrical switch. This switch architecture is scalable but the main constraint is the requirement of a large number of optical components. We have not discussed the power budget analysis for architectures A2 and A3 because the analysis and calculation procedures will remain same as for A1. The only change will occur in the final values of maximum allowed circulations, since each of these architectures incorporates different optical components.

Chapter 8

A comparative analysis of Optical Packet Switch Architectures for Optical Cost and Bursty Traffic

In this chapter, we present the comparative analysis of various optical packet switch architectures[1]. The comparison is done on the basis of optical cost of these switch architecture and their performance for bursty traffic. The architectures chosen for the analysis have already been discussed in the earlier chapters. This chapter should be considered as the cumulative extension of the previous ones.

8.1 Switch Architectures - an overview

The architectures chosen for comparison, are the Staggering Switch [28], its modified version (Chapter 3) [58], feedback shared buffer switch architecture (Chapter 5) [62] and feed-forward shared buffer switch (Chapter 7) [60]. These architectures are referred as A1, A2, A3 and A4 respectively in the following text. These are shown in Figures 8.1 to

[1] "Optical Packet Switch Architectures: A comparative analysis for Bursty Traffic and Optical Cost," *Fiber and Integrated Optics*, (accepted for Nov/Dec' 2007 Issue).

8.4. All of these are examples of "almost-all" optical packet switches incorporating fiber delay lines for contention resolution. These architectures extract the header information from the packets, process it electronically, and route the packets following the scheduling algorithm defined for the respective architectures. The details of these architectures have already been given in the respective chapters. Here, we will present only the comparative analysis. We are using the notations 'S' and 'R' instead of 'm' and 'D' respectively for A1 and A2, as used in Chapter 3. This is done to avoid the confusion, because the notations 'm' and 'D' are also being used for A3 and A4.

We will first compute the optical cost of the above mentioned four architectures. Then, depending upon the similar range of optical cost, the performance of these architectures will be compared for bursty traffic.

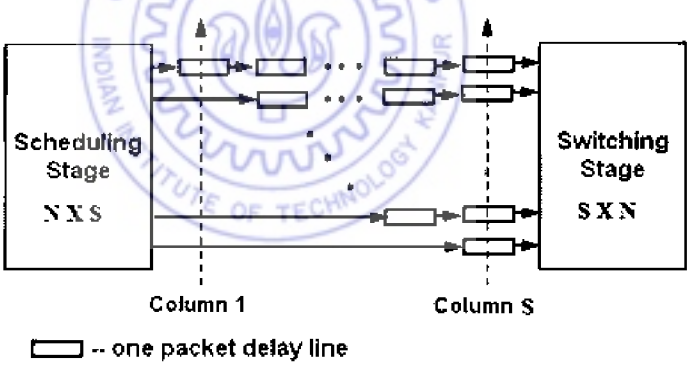


Figure 8.1: Switch Architecture - A1.

8.2 Optical cost analysis

The cost estimation for any switch architecture consists of investigation of optical cost as well as electronic cost [9]. The optical cost estimation deals with the count of optical components used to build that architecture, whereas the electronic cost is obtained by counting the number of optical-electronic-optical (OEO) conversion circuits used for

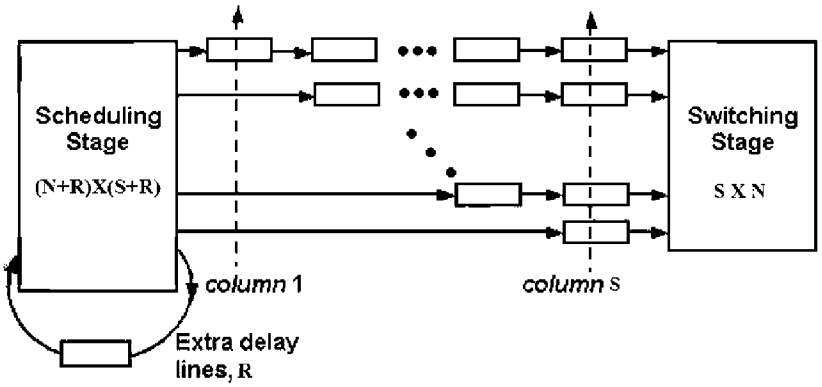


Figure 8.2: Switch Architecture - A2.

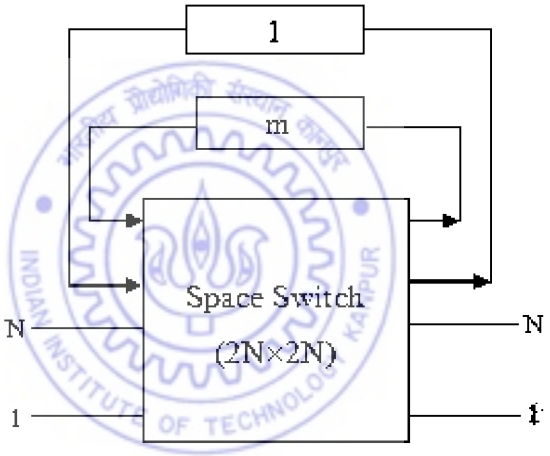


Figure 8.3: Switch Architecture - A3.

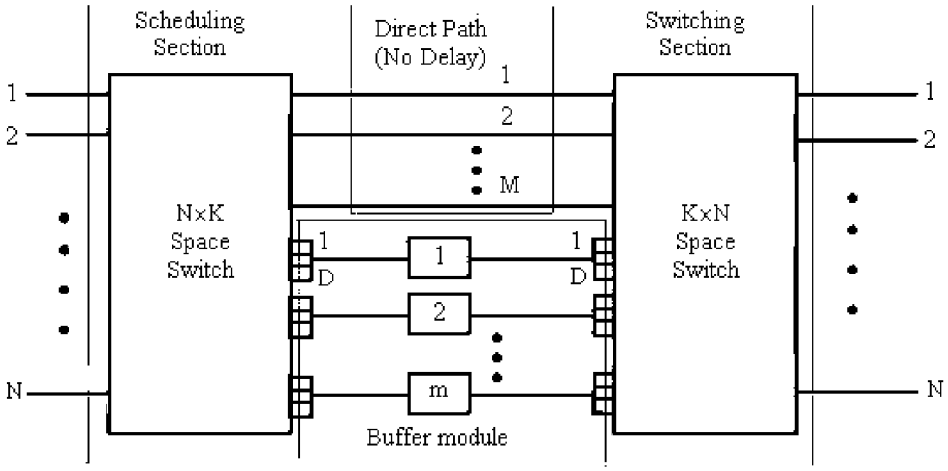


Figure 8.4: Switch Architecture - A4.

header reading. The architectures considered here use various techniques to resolve the contention among the packets and hence, they incorporate different sets of optical components. In this chapter, we compare only their optical costs because the header reading process is assumed to be the same for each architecture. Thus, their electronic cost will also remain same.

The optical cost of a switch architecture is calculated by adding the optical cost of individual optical components used in that architecture. The optical cost of individual optical components is obtained by counting the number of fiber-to-chip couplings (FCC) [9]. The FCC is the number of interconnections to the outer world through that component. The counting of optical components in the switch architecture is started from the switch input. The number of each component is multiplied by the respective number of FCCs as given in Table 8.1, and then the optical cost of the whole switch is calculated by adding them.

Function	**Description**	**Number of FCC**
$C_D(W)$	Demultiplexer (W channels)	$W+1$
$C_T(W)$	TWC (W wavelength)	$W+1$
$C_{Com}(W)$	Combiner ($W \times 1$)	$W+1$
$C_{Switch}(I,O)$	Switch (I/O input/output ports)	$I+O$
C_{Amp}	Amplifier	2
C_{ISO}	Isolator	2
C_{BPF}	Band Pass Filter	2
C_{3dB}	3dB Coupler	4

Table 8.1: Optical cost function of the components

8.2.1 Estimation of Optical cost

In this section, we will compute the optical cost of each architecture, and then decide which of these should be compared.

8.2.1.1 Optical cost of architecture A1

The optical cost for A1 is calculated in term of FCCs as

$$C_{A1} = C_{Scheduling\ section}(N,S) + C_{Switching\ section}(S,N)$$

Since we are using the switch A1 with $N = 16$ and $S = 16$, then C_{A1} will be calculated from the parametric values of Table 8.1 as,

$$C_{A1} = (N+S) + (S+N) = 2N + 2S = 64$$

8.2.1.2 Optical cost of architecture A2

The optical cost for A2 is calculated in term of FCCs as

$$C_{A2} = C_{Scheduling\ section}(N+R, S+R) + C_{Switching\ section}(S,N)$$

Using the parameters for A1 alongwith $R = 4$, the optical cost for A2 is obtained as

$$C_{A2} = (N+R+S+R) + (S+N) = 2N + 2S + 2R = 72$$

8.2.1.3 Optical cost of architecture A3

The optical cost for A3 is calculated in term of FCCs as

$$\begin{aligned} C_{A3} &= C_{Switch}(2N,2N) + m \times [D \times C_T(B) + C_{Com}(D) + C_{3dB} + C_D(B) \\ &\quad + B \times C_T(D) + C_{Com}(B) + C_{Amp} + C_{ISO} + C_D(D)] \\ &= (2N+2N) + m \times [D \times (B+1) + (D+1) + 4 + (B+1) \\ &\quad + B \times (D+1) + (B+1) + 2 + 2 + (D+1)] \end{aligned}$$

We are using the switch A3 of $N = 16$ with $m = 4,\ B = 8$ and $D = 4$. Thus the optical cost of A3 is

$$C_{A3} = 4N + m \times [2BD + 3D + 3B + 12] = 512$$

8.2.1.4 Optical cost of architecture A4

The optical cost for A4 is calculated in term of FCCs as

$$\begin{aligned} C_{A4} &= C_{Switch}(N,K) + m \times [D \times C_T(B) + C_{Com}(D) + C_{3dB} + C_D(B) \\ &\quad + B \times C_T(D) + C_{Com}(B) + C_{Amp} + C_{ISO} + C_{BPF} + C_D(D)] \\ &\quad + C_{Switch}(K,N) \\ &= (N+K) + m \times [D \times (B+1) + (D+1) + 4 + (B+1) \\ &\quad + B \times (D+1) + (B+1) + 2 + 2 + 2 + (D+1)] + (K+N) \end{aligned}$$

We are using the switch A4 of $N = 16$ with $m = 4,\ B = 8,\ D = 4$ and $M = 16$. We have considered $M = 16$ for A4 to make it equivalent to the lower N output ports of A3 for direct transfer of packets without being stored. Since $K = M + m \times D = 32$, the effective size of the scheduling and switching stages of A4 will be 16×32 and 32×16 respectively. Thus the optical cost of A4 is

$$C_{A4} = 2N + 2K + m \times [2BD + 3D + 3B + 14] = 552$$

We found that the optical costs of A1 and A2 are nearly equal, so they are comparable. Similarly, the optical costs of A3 and A4 are in same range, so they are also comparable. While, the optical costs of A3 and A4 are much greater than that of A1 and A2, so the comparison between them is not justified.

8.3 Bursty traffic analysis

Bursty traffic is more realistic, and has been considered for comparing the switch performance. For this analysis, we have considered two-states Markov chain model to describe the behavior of bursty data. Further, the traffic is assumed to be uniformly distributed in terms of destination. The architectures A1, A2, A3 and A4 are simulated and analyzed for bursty traffic arrival to obtain packet loss probability and average delay.

8.3.1 Bursty traffic model

The traffic on each input will be composed of bursts of packets destined to the same output. These bursts are followed by an idle period which can also be of length zero, where the new burst will be adjacent to the older one i.e., two back to back bursts (Figure 8.5). The bursty traffic is characterized by two parameters:

1. average offered traffic load (ρ), and
2. average burst length (BL).

Time correlation of traffic on each input can be modelled by the Markov chain as shown in Figure 8.6. The chain is composed of two states: idle state (0) or burst state (j). The system will be in the idle state when no packet arrives in the current slot. Also, no packet will arrive in the next slot with probability P_a. Thus, a new burst will begin with probability $(1 - P_a)$ and the system will be transferred to the burst state 'j' where j is the destination. We have assumed that j can choose any integral value between 1 to N with equal probability for an $N \times N$ switch. The next arrival will be either the

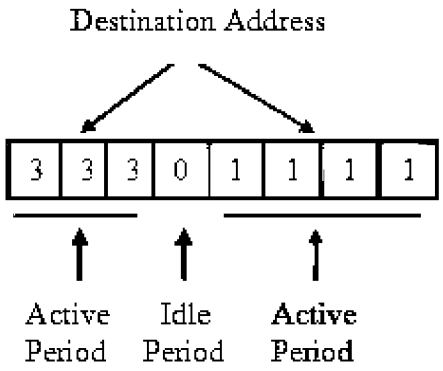


Figure 8.5: Packet sequencing for bursty traffic

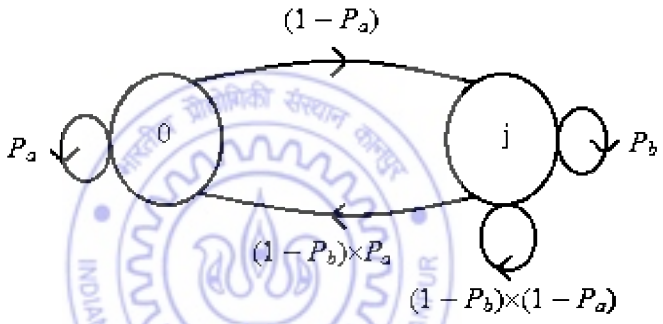


Figure 8.6: Markov chain model for bursty traffic

part of existing burst with probability P_b (i.e., destined to the same destination) or the burst will terminate with probability $(1 - P_b)$. The termination of the burst can occur in two ways.

1. Either a new burst will start for another destination. This transfers the system to a new bursty state with different value of j. The choice of another destination is equiprobable. The probability of going to this state from the existing burst state will be $(1 - P_b) \times (1 - P_a)$.

2. Or, the transition to idle state with probability $(1 - P_b) \times P_a$.

The steady state equation for this Markov chain (Figure 8.6) can be written in terms of steady state probabilities as,

$$\begin{bmatrix} P_a & (1-P_b)P_a \\ (1-P_a) & (1-P_b)(1-P_a)+P_b \end{bmatrix} \begin{bmatrix} \pi_0 \\ \pi \end{bmatrix} = \begin{bmatrix} \pi_0 \\ \pi \end{bmatrix} \tag{8.3.1}$$

Here, π is the steady state probability of the system being in any one of states j i.e.,

$$\pi = \sum_{j=1}^{N} \pi_j \tag{8.3.2}$$

Further, using the property that summation of all the state probabilities of any Markov chain is equal to unity i.e.,

$$\pi_0 + \pi = 1, \tag{8.3.3}$$

By solving Equations 8.3.1 and 8.3.3, we get the steady state probabilities in term of P_a and P_b, as

$$\pi_0 = \frac{P_a(1-P_b)}{1-P_aP_b} \tag{8.3.4}$$

and

$$\pi = \frac{(1-P_a)}{1-P_aP_b} \tag{8.3.5}$$

The average offered traffic load ρ will be equal to the fraction of the time the system is not in the idle state i.e.,

$$\rho = 1-\pi_0 = \frac{(1-P_a)}{1-P_aP_b} \tag{8.3.6}$$

The probability of burst length being k is

$$P(k) = (1 - P_b)P_b^{k-1}, \quad k \geq 1 \tag{8.3.7}$$

Hence the average burst length is

$$BL = \sum_{k=1}^{\infty} kP(k) = \frac{1}{1 - P_b}. \tag{8.3.8}$$

Considering some fixed value of ρ and BL in Equations 8.3.6 and 8.3.8 respectively, the value of P_a and P_b can be calculated. This analysis is used to simulate the performance of various switch architectures (Figure 8.1 to 8.4) under bursty traffic conditions. The results are analyzed and plotted in the following section.

8.3.2 Performance evaluation and Results

According to the results of optical cost analysis, we will compare A1 with A2, and A3 with A4, with respect to the performance under bursty traffic.

8.3.2.1 Comparison of A1 and A2

The simulation results for packet loss probability and average delay for the architecture A1 of size $N = 4,\ S = 4$ have been obtained under the bursty traffic arrival pattern of various burst lengths. The effect of increasing the number of extra delay lines (R) for A2 on these results are shown in Figure 8.7 and 8.8. The loss probability is better for $R = 4$ as compared to $R = 0$ when the length of bursty traffic (BL) is increased from 1 to 5. Also, the effect of increasing R is more pronounced for smaller lengths of burst (Figure 8.7). It should be remembered that when $R = 0$, the architecture A2 becomes

similar to A1. The average delay for a packet in A2 is more for large burst lengths on all the loads (Figure 8.8). But for smaller burst lengths and lower loads, the average delay in A2 is same as in A1. These results are expected because the packets, arriving in the form of burst, have to wait for longer duration before being serviced.

The effect of various combination of S and R at a particular burst length of $BL = 2$ and switch of size $N = 4$ are shown in Figure 8.9 and 8.10. The loss probability is comparable for $(S, R) = (4, 2)$ and (6,0) while the results are better for the case of $(S, R) = (4, 4)$ as compared to (6,0). The average delay variation for $(S, R) = (6, 0)$ lies between $(S, R) = (4, 2)$ and (4,4). The reason behind getting these results is related to the effective buffer utilization, and has been already discussed in the section 3.3.1.

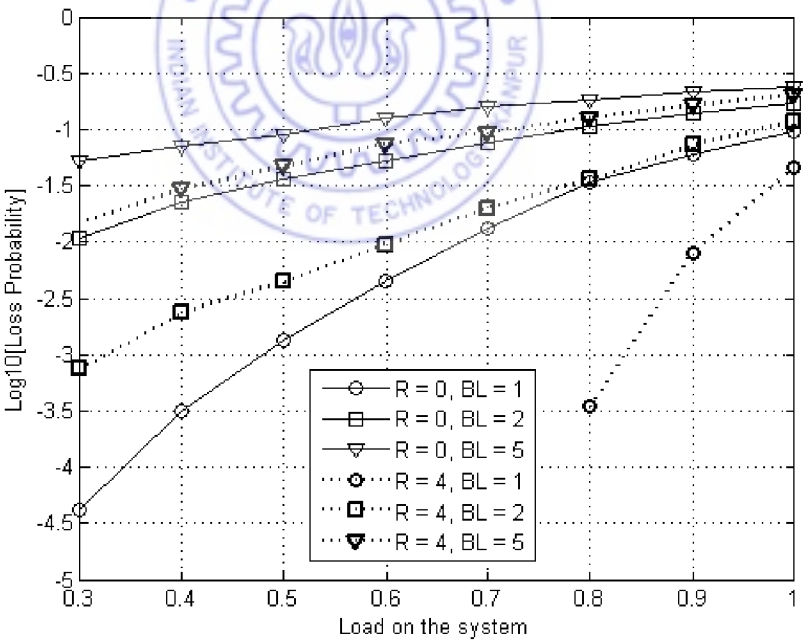


Figure 8.7: Loss probability for various length of bursty traffic applied on switch of $N = 4$ and $S = 4$. A1 is represented by $R = 0$ while $R = 4$ is used for A2

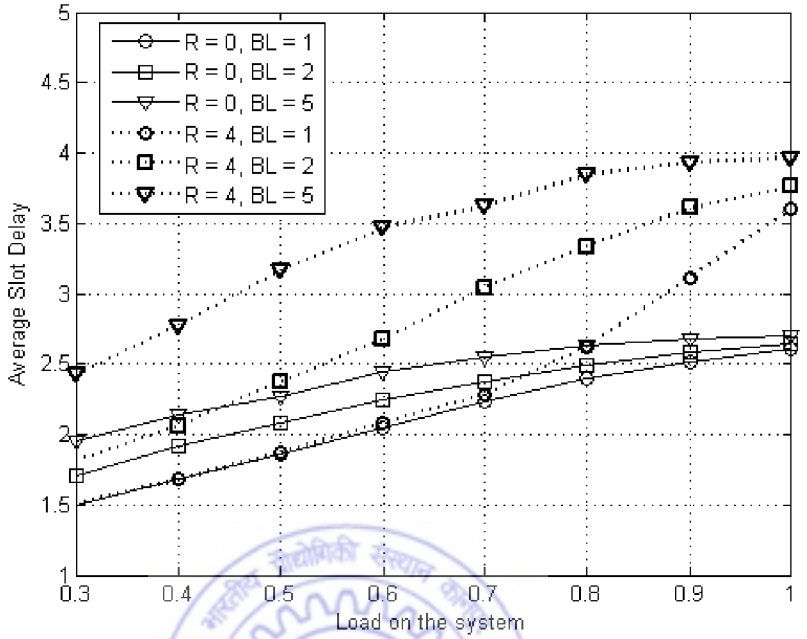


Figure 8.8: Average delay for various length of bursty traffic applied on switch of $N = 4$ and $S = 4$. A1 is represented by $R = 0$ while $R = 4$ is used for A2

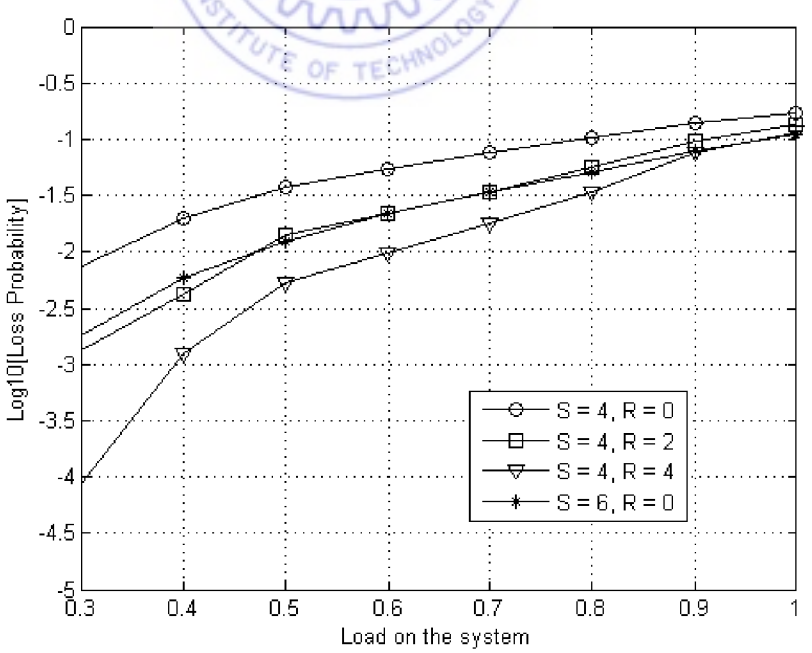


Figure 8.9: Comparison of Loss probability using various combination of S & R for $BL = 2$

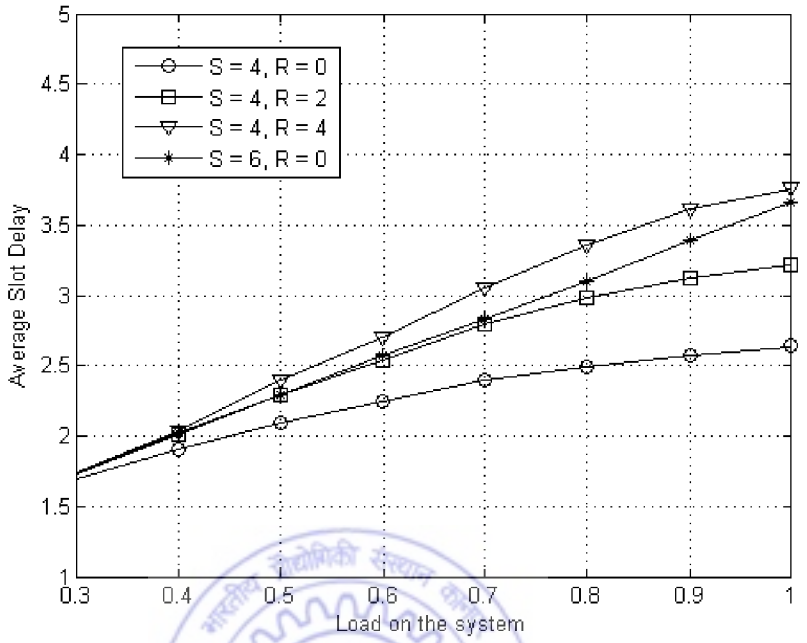


Figure 8.10: Comparison of Average delay using various combination of S & R for $BL = 2$

8.3.2.2 Comparison of A3 and A4

The bursty traffic analysis for A3 and A4 is done for same buffering capacity with $N = 16,\ m = 4,\ B = 8$ and $M = 16$. We have considered $M = 16$ for A4 as it is equivalent to the lower N output ports of A3 for direct transfer. The loss probabilities (Figure 8.11) and the average delay (Figure 8.12) are better for A3 as compared to A4 under all the considered burst lengths. Usually, the average delay increases when loss probability is reduced by increasing the resources, but this is not happening with A3. It implies that A3 is effectively utilizing the available buffering capacity while A4 is not doing so.

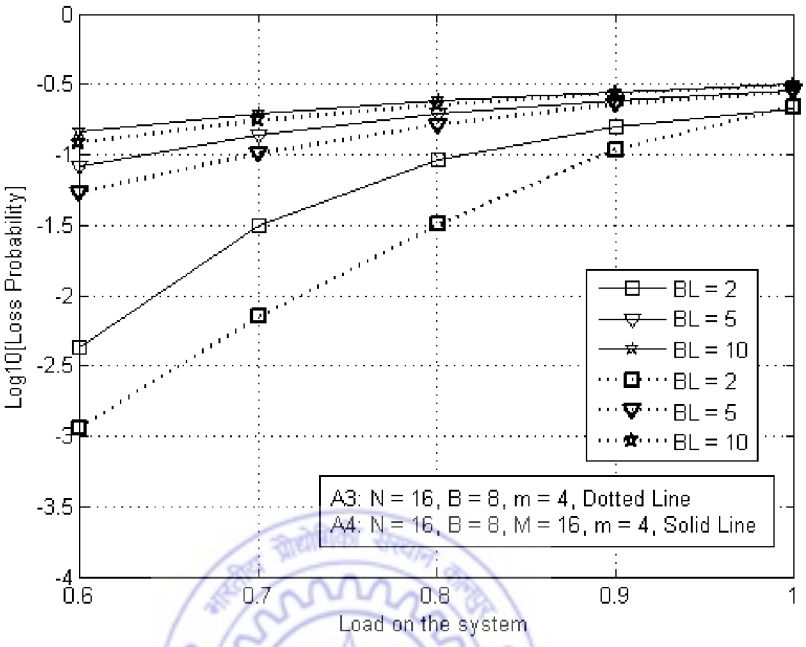


Figure 8.11: Loss probability for Feedback switch (A3) and Feed-forward switch (A4).

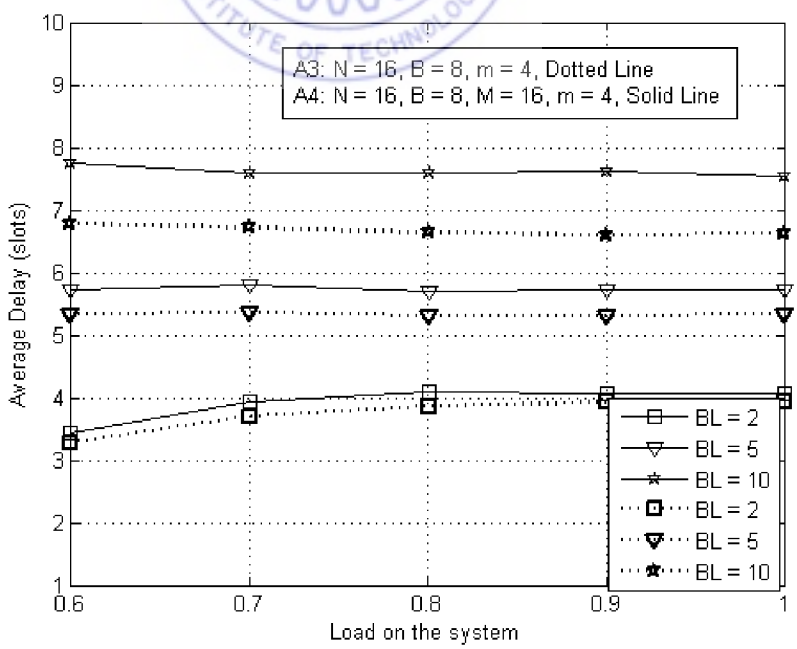


Figure 8.12: Average delay for Feedback switch (A3) and Feed-forward switch (A4).

8.4 Summary

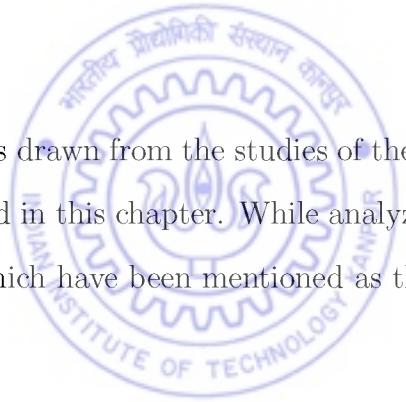
The modified staggering switch is advantageous over the original one, in terms of loss probability under bursty traffic. The optical cost of A2 is also not much greater than that of A1.

The feed-forward switch A4 effectively uses the principle of staggering switch A1 and in addition, it applies the WDM technique to store the packets in the recirculating loop. Due to their much higher optical cost, A3 and A4 are not compared with A1 and A2. Also, the FIFO discipline cannot be maintained in A1 and A2 while A3 and A4 maintain it.

The architecture A3 utilizes WDM loop buffer modules in feedback configuration for data storage while the architecture A4 utilizes WDM loop buffer modules in feed-forward configuration. The optical cost of A3 is much higher but still comparatively less than A4, and so A3 is compared with A4. The feedback switch is advantageous over feed-forward in term of loss probability and average delay under bursty traffic due to its more effective use of buffers. Hence we can conclude that the feedback shared buffer switch architecture (A3) is best option among all the compared architectures in this chapter.

Chapter 9

Conclusions and Scope for Future Work



The general conclusions drawn from the studies of the switch architectures presented in this thesis are presented in this chapter. While analyzing the work, some new problems have been identified which have been mentioned as the possibility for future work.

9.1 Conclusions

The general conclusions of the thesis are as follows. All optical switches (that do not perform deflection in space or wavelength domains) require optical buffers for storage of those packets which are going to be lost, and thus improve the loss probability performance. Fiber delay lines are a viable option for implementing optical buffers. The length of these delay lines is generally considered to be equal to one time slot or one packet length. We have observed a trade-off between loss probability and average delay in all the architectures.

We have proposed addition of extra delay lines to the Staggering Switch architec-

ture. It does not affect the cost of the architecture greatly. Further, this slight increase in cost is overshadowed by the performance improvement in terms of lower probability of packet loss. In the Data Vortex switch architecture, a modification has been suggested which improves the performance while retaining the switch scalability.

In all the proposed loop buffer based architectures, the application of modular structure reduces the need of a large range of wavelengths because the same set of wavelengths is used in all the buffer modules. The multiple loop buffer modules act together as one single fully shared buffer. The use of loop buffer module is a better choice because it provides WDM shared buffering, and its capacity can be increased without changing the actual size of the switch architecture.

The presence of various optical components in the loop buffer generates several noise components. This imposes a limit on the number of maximum allowed circulations. Using the power budget analysis, the recirculation limits were computed. This circulation limit is then used to obtain the packet loss probability as well as the average delay through the switch using simulations. These simulation results have been validated by comparing them with the mathematical results. Then, these results have been used to gain the understanding of the proposed optical packet switch architectures' performance. All the switch architectures discussed here perform well under uniform random traffic as well as the bursty traffic conditions.

In all the proposed architectures, we have considered the single switch network which implies that the fresh data is generated at the switch input and received at the switch output. In a network where many such switches will be cascaded, packet may go through different amount of circulations in different switches. The packet will be passed through similar core switches many times (i.e., whenever it moves from one switch to

other). Further, the links between these switches will also attenuate the signal. Thus, the signal will have to suffer loss from the additional core switches and the fiber links. Hence, the number of maximum allowed circulations will be decreased and will depend on history of the packet. The history of a packet will refer to the number of circulations already done at the previous nodes, before reaching any particular node. So, the total amount of circulations a packet performs in all the switches have to be less than the number of maximum allowed circulations in case of a single switch network. In order to simplify and to focus only on the single switch performance, we have taken this maximum limit.

9.2 Scope for Future Work

During the course of this work, we have identified some problems which need further investigations.

1. Performance analysis of the switches, under more realistic traffic (e.g., Pareto), should be done. The effective utilization of buffer need to be investigated. The lessons learned from these investigations may be used for better design of switch architectures [27, 67].

2. Analyses of these architectures when variable length packets are used needs to be done. The investigations will provide insight in deciding the optimal length of the loop buffer [10].

3. The performance of the network built by cascading several such switches needs to be evaluated. The current thesis assumes single node network. This also needs a framework where link degradation and switch degradation needs to be

characterized in terms of equivalent number of recirculations.

4. The degradation in the signal quality may demand for the regeneration of a signal. When different kind of regenerations are used, one needs to understand the limitations of networks having all optical packet switches.

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1. **Rajat Kumar Singh**, Rajiv Srivastava and Yatindra Nath Singh, "Feed-forward and shared buffer based optical packet switch architecture," *Optical Switching and Networking*, (under review).

2. **Rajat Kumar Singh**, Rajiv Srivastava and Yatindra Nath Singh, "AWG and EDFA based Optical Packet Switch using Feedback Shared Loop Buffer Memory," *Optical and Quantum Electronics*, (under review).

3. Rajiv Srivastava, **Rajat Kumar Singh** and Yatindra Nath Singh, "Fiber Optic Loop Buffer Switch: Modeling, Analysis and Simulation," *Fiber and Integrated Optics*, (under review).

4. Rajiv Srivastava, **Rajat Kumar Singh** and Yatindra Nath Singh, "WDM Based Optical Packet Switch Architectures," *Journal of Optical Networking*, (under review).