# WDM Fiber Delay Line Based Optical Packet Switch Architectures 



# WDM Fiber Delay Line Based Optical Packet Switch Architectures 

A Thesis Submitted<br>in Partial Fulfilment of the Requirements

for the Degree of
DOCTOR OF PHILOSOPHY

to the

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY KANPUR


## CERTIFICATE

It is certified that the work contained in the thesis entitled "WDM Fiber Delay Line Based Optical Packet Switch Architectures" being submitted by Mr. Rajiv Srivastava has been carried out under my supervision. In my opinion, the thesis has reached the standard fulfilling the requirement of regulation of the $\mathrm{Ph} . \mathrm{D}$. degree. The meult embodied in this thesis have not been submitted elsewhere for the award of any degree or diploma.

12 Nov., 2008

## Synopsis

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| Department | $:$ | Electrical Engineering |
| Thesis Title | $:$WDM Fiber Delay Lines Based <br> Optical Packet Switch <br> Architectures |  |
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| Month and year of submission | $:$ Nov., 2008 |  |

The demand for higher bandwidth is increasing day by day due to the data centric application like, Internet TV, video-on-demand etc.. One of the technology which may be useful when building networks to cater to this increasing demand, is optical packet switching. The optical packet switching technology is considered as next generation data transfer technology because of its high throughput, low latency, fine granularity and ultimate bandwidth utilization. The optical network implementations are composed of switches which can be electronic or all-optical. The switching aims to route the packet to the destined output port. One of the key issues involved in optical networking is the design of switch/router architectures which can perform the switching operation efficiently at high data rates [46]. With current technology, optical processor is not feasible therefore hybrid approach where data propagates in optical domain and control operations are performed by the electronics is adopted in the experimental studies. It is referred to as photonic packet switching technology. The important aspects of photonic
packet switching are clock recovery, packet synchronization, packet header replacement, packet routing, contention resolution and control [13, 66]. Contention is one of the key issues, which occurs when two or more than two packets try to leave the switch from the same output port at the same time. To avoid the contention, one of the contending packets, is directed to the intended output port and rest of them are either stored or dropped. All-optical memory suitable for optical storage, is not currently possible due to the technological limitations. Therefore, deflection routing or optical fiber delay lines (in traveling or re-circulating type configuration) can be used as an alternative. Different solutions for optical buffering by using fiber delay lines have evolved in last few years $[5,25,26,56]$ and researcher are still trying to obtain better solutions. Optical buffering can be introduced in three ways: input buffering, output buffering and shared buffering $[2,11,24,54]$. Output and shared buffering are most frequently used in the switches.

In this thesis, different aspects of optical buffering are investigated in various optical packet switch architectures. New architectures have also been proposed along with the novel buffering structure. The main objective of the thesis is to identify the limitations of the loop buffer based architectures and to solve them by proposing new architectures which have simpler buffer structure such that large number of packets can be stored in the buffer with very few components.

The thesis has been organized in the following eight chapters.
Chapter 1 explains the evolution of fiber optic communication and optical networks. This chapter discusses the fundamental issues of photonic packet switching like Control, Packet routing, Packet synchronization, Contention resolution, and Packet header replacement. The overview of the different class of optical packet switch architectures is presented. The various aspects of the switch design as well as description of the optical
components are presented. Finally, performance evaluation parameters like BER and packet loss probability are discussed.

Chapter 2 discusses four optical loop buffer based architectures classified as A1, A2, A3 and A4. In this chapter, two new architectures are presented, where in the buffer, SOA gates are replaced by TWCs which facilitate functionalities like, simultaneous read/write operation and dynamic wavelength re-allocation etc.. The effectiveness of modification, has also been verified through simulation [63].

Chapter 3 explores the architecture A2 which was found to perform better than other architectures presented in chapter 2, in terms of physical layer impairments. In this chapter, a mathematical model is presented to obtain maximum number of allowed recirculations of the data at different power levels. In the modeling, detrimental effect of ASE noise and FWM is considered. Finally, bounded regions are drawn for the proper operation of the architectures.

In Chapter 4, placement of the regenerators inside the buffer is proposed to further improve the performance of architecture A2. An expression is presented to evaluate the required number of regenerators that have to be placed in the buffer for different buffer capacities and circulation limits, such that full buffer capacity can be utilized without any circulation limits. Simulation results are presented to verify the hypothesis.

In Chapter 5, two multi-wavelength optical packet switches are presented which have large storage capability. The first of these two architectures, A6 [62] utilizes the simultaneous wavelength conversion capability of the TWCs, and thus allows large storage capacity. In the architecture A7 [61], buffer is created using segments of fiber and fiber Bragg gratings only. Use of the FBG in the buffer can set a new direction in optical packet switch architectures because of its large wavelength scalability, low insertion loss and dispersion reduction capability. These two architectures have potential to perform better than earlier discussed architectures under bursty traffic condition where large
buffer space will be required to obtain low packet loss probability.
The architecture proposed in chapter $\mathbf{6}$ is realized using components like optical reflectors, tunable wavelength converters (TWCs), arrayed waveguide gratings (AWGs) and segments of fiber. This architecture uses routing pattern of AWG, and its symmetric nature, to simplify switch operation significantly. It is also shown that using multi-wavelength optical reflectors, length of delay lines can be reduced to half of their original value. In the presented architecture, large number of packets can be stored in a single fiber delay lines and in the buffer, control of the any device is not required. In the proposed architecture, these limitations are eased as buffer can be created by using only very few components.

In Chapter 7, cost estimation of the different architectures discussed in the thesis, is presented. The cost analysis of the architectures is done using FCC method. For the cost of the TWCs, various models have been considered. In chapter 7, it was found that architecture A7 and architecture A8 have lower cost than all other considered architectures.

Chapter 8 discusses the major conclusions of the thesis, and suggest problem that can be part of further study.

## Dedicated to my Family, Teachers and Friends

## Acknowledgements

People prefer to follow those who help them, not those who intimidate them.

- C. Gene Wilkes

I feel immense pleasure in expressing my profound sense of gratitude to my thesis supervisor Dr. Y. N. Singh under whose supervision and inspiring guidance, I had privilege to carry out my research work. I am indebted to him for his constant and ungrudging encouragement, valuable suggestions and ingenious ideas. Words won't be sufficient to quantify his immense knowledge and understanding of the subject which has helped me in better understanding of theoretical aspects of differential equations in abstract space, in particular. He showed me different ways to approach a research problem and the need to be persistent to accomplish any goal.

I express my heartiest thanks to prof. P. K. Kalra, Head of the Department of Electrical Engineering, IIT Kanpur for providing me necessary facilities. I am also grateful to all the faculty members for their support and encouragement.

I immensely express my heartiest thanks to my friends Anupam, Ashutosh, Harshita,

Praveen, Sivli, Ramesh, Tathagata and Tony for their support and help. I have spent some of the craziest and most memorable moments with them. I would like to acknowledge my family members whose continuous support and love helped me carry out my work.

I would also like to acknowledge my friend Rajat Kumar Singh whose valuable suggestion and discussion, helped me in my work.

I wish to express my deep gratitude to my all the teachers whose consistent help and encouragement to boost my moral and confidence.

Though it is beyond the scope of any acknowledgement for all that I have received from my parents Mr. D. K. Srivastava and Mrs. Indra Srivastava, by the way of inspiration, patience and encouragement at all times but most conspicuously during this period, yet I make an effort to express my heartfelt and affectionate gratitude to them. May God guide me to the wishes of my parents so that they feel the joy of having lived a contained life in my conduct to them.
(Rajiv Srivastava )

## Acronyms and Abbreviations

| AO | Acousto-Optic |
| :--- | :--- |
| OADM | Optical Add/Drop Multiplexer |
| ASE | Amplified Spontaneous Emission |
| ATM | Asynchronous Transfer Mode |
| AWG | Arrayed Waveguide Grating |
| BER | Bit Error Rate |
| BPF | Band Pass Filter |
| CW | Continuous Wave |
| CWDM | Course Wavelength Division Multiplexing |
| DSF | Dispersion Shifted Fiber |
| DWDM | Dense Wavelength Division Multiplexing |
| DXC | Digital Cross-Connect |
| EDFA | Erbium Doped Fiber Amplifier |
| FDLs | Fiber Delay Lines |
| FBGs | Fiber Bragg Gratings |
| FCC | Fiber-to-Chip Coupling |
| FIFO | First in First out |
| FF | Fixed Filter |
| FWM | Four Wave Mixing |
| IEEE | Institute of Electrical and Electronics Engineers |
| ITU | International Telecommunication Union |
| ISI | Inter Symbol Interference |
| KEOPS | Keys to Optical Packet Switching |
| LEDs | Light Emitting Diodes |
| LASER | Light Amplification by Stimulated Emission and Radiation |
| NDF | Non-Zero Dispersion Shifted Fiber |
| OADM | Optical Add-Drop Multiplexer |
| OEO | Optical-Electronic-Optical |
| OLS | Optical Label Switching |
|  |  |


| OLB | Optical Loop Buffer |
| :--- | :--- |
| OBS | Optical Burst Switching |
| OPS | Optical Packet Switching |
| OXC | Optical Cross Connect |
| PLR | Packet Loss Rate |
| PON | Passive Optical Network |
| PSTN | Public Switched Telephone Network |
| RAM | Random Access Memory |
| SBS | Stimulated Brillouin Scattering |
| SLOB | Switch with Large Optical Buffer |
| SNR | Signal to Noise Ratio |
| SPM | Self Phase Modulation |
| SRS | Stimulated Raman Scattering |
| SOA | Semiconductor Optical Amplifier |
| TDM | Time Division Multiplexing |
| TDL | Tunable Delay Line |
| TF | Tunable Filter |
| TWC | Tunable Wavelength Converter |
| WASPNET | Wavelength Switched Optical Network |
| WDM | Wavelength Division Multiplexing |
| WSU | Wavelength Speed-Up |
| WADM | Wavelength Add/Drop Multiplexer |
| WWDM | Wide Wavelength Division Multiplexing |
| XGM | Cross Gain Modulation |
| XPM | Cross Phase Modulation |

## List of Symbols

| $R$ | Responsivity |
| :--- | :--- |
| $n_{s p}$ | Population Inversion Factor |
| $G$ | Gain of the Amplifier |
| $\nu$ | Frequency |
| $\lambda$ | Wavelength |
| $K$ | Circulations |
| $b$ | Bit |
| $N$ | Switch Size |
| $B$ | Buffer size |
| $M$ | Modules |
| $L$ | Length |
| $n$ | Refractive Index |
| $B_{R}$ | Bit Rate |
| $G_{p}$ | Group |
| $S$ | Sets |
| $\rho$ | Load |
| $R_{b}$ | Regenerators |
| $W$ | Wavelengths |
| $b_{n}$ | Number of Bits |
| $h$ | Planck Constant |
| $c$ | Speed of Light |
| $\epsilon$ | Extinction Ratio |
| $B_{e}$ | Electrical Bandwidth |
| $B_{o}$ | Optical Bandwidth |
| $q$ | Electronic Charge |
| $P_{s}(1)$ | Power for Bit One |
| $\chi_{n}$ | Third order nonlinear susceptibility |


| $R_{L}$ | Load Resistance |
| :--- | :--- |
| $T$ | Temperature |
| $K_{B}$ | Boltzmann Constant |
| $A_{3 d B}$ | Loss of 3 dB Coupler |
| $A_{\text {Com }}$ | Loss of the Combiner |
| $A_{\text {Splitter }}$ | Loss of the Splitter |
| $A_{\text {Demux }}$ | Loss of the Demux |
| $A_{T W C}$ | Loss of the Tunable Wavelength Converter |
| $A_{s}$ | Splice Loss |
| $A_{F}$ | Loss of the Fiber |
| $A_{\text {Iso }}$ | Loss of the Isolator |
| $A_{\text {Cir }}$ | Loss of the Circulator |
| $\gamma$ | Scattering Loss |
| $\Gamma$ | Confinement Factor |
| $P_{p}$ | Pump Power |
| $\chi$ | Conversion Efficiency |
| $A_{F B G}$ | Loss of Fiber Bragg Gratings |
| $A_{B P F}$ | Loss of Band Pass Filter |
| $A_{F F}$ | Loss of Fixed Filter |
| $A_{T F}$ | Loss of Tunable Filter |
| $A_{\text {AWG }}$ | Loss of Arrayed Waveguide Grating |
| $A_{\text {in }}$ | Loss of Input Unit |
| $A_{\text {out }}$ | Loss of Output Unit |
| $A_{\text {loop }}$ | Loss of Loop Buffer |
| $A_{\text {eff }}$ | Effective Area of the Fiber |
| $\Delta \lambda$ | Source Spectral Width |
| $\|D\|$ | Second Order Dispersion Coeffiecent |
| $C_{T W C}$ | Cost of the Tunable Wavelength Converter |
| $C_{\text {Demux }}$ | Cost of the Demux |
| $C_{S p l i t e r ~}$ | Cost of the Splitter |
| $C_{\text {Combiner }}$ | Cost of the Combiner |
| $C_{M u x}$ | Cost of the Multiplexer |
| $C_{S w i t c h / A W G}$ | Cost of the Switch/AWG |
| $C_{E D F A}$ | Cost of the EDFA |

$C_{B P F}$ Cost of the Band Pass Filter
$C_{\text {Iso }} \quad$ Cost of the Isolator
$C_{3 d B} \quad$ Cost of the 3 dB Coupler
$C_{F} \quad$ Cost of the Fiber
$C_{S O A}$ Cost of SOA
$C_{F B G}$ Cost of the Fiber Bragg Grating
$C_{F F} \quad$ Cost of the Fixed Filter
$C_{T F} \quad$ Cost of the Tunable Filter
$C_{O r} \quad$ Cost of the Optical Reflector

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## Chapter 1

## Introduction

### 1.1 Introduction

Communication is a process that allows living being to exchange information. In human beings this implies exchange of thoughts, ideas etc.. In pre-historic time, for the information sharing, smoke signals, fire signals, drums etc. were used. But these processes were suitable for communication over small distances. Necessity of information transfer over the long distances gave birth to new era of modern communication processes. In modern times, the process of sending the information bearing signals over a distance for the purpose of communication is referred to as 'telecommunication'. The word telecommunication include telephony, telegraphy, television and data communication.

The foundation of the modern telecommunication was laid by the invention of the telegraphy in 1837 [39]. The first telegraph link was deployed from Baltimore to Washington. The modern telecommunication took off with the invention of telephone in 1874 by Alexander Graham Bell [3]. However, the trans-continental telephony came into existence in 1913. The invention of transistor in 1948 was the major breakthrough for the modern telephony systems and soon after that compact telephones came into
existence. The evolution of the telephone system gave rise to the world's public circuitswitched telephone networks popularly known as PSTN (Public Switched Telephone Network). Traditional PSTN systems were circuit switched in nature and transmission medium was copper cables. With the advances in optical fiber, a new era in transmission technology evolved, because optical fibers offer much higher bandwidths and are less susceptible to various kinds of electromagnetic interferences and other unwanted effects.

### 1.2 Evolution of Optical Fibers

The development of fiber optic technology provided the required medium for guided transmission of light. The all-glass fiber was first used by Brian O'Brien at the American Optical Company in his fiberscope, the image-transmitting device, during 1950s. However, this fiber was without cladding. Therefore, these fibers have large optical loss. Soon after that, optical fibers with cladding were developed. During the same time period, extensive research was going on in the field of lasers and LEDs (light emitting diodes). In 1957, the idea of using lasers in fiber optics as a source for transmission of signals was given by Gordon Gould at Columbia University and after some time by Charles Townes and Arthur Schawlow at Bell Laboratories. The invention of semiconductor lasers in 1962 opened the way for optical fiber communication. These lasers were the most suitable ones for use in optical fiber communication. At the time when fiber losses were more than $1000 \mathrm{~dB} / \mathrm{km}$, two scientists Dr Charles Kuen Kao and Dr. George Hockham were working at the Standard Telecommunication Laboratory in England. In 1966, they suggested in their landmark paper [33] that if the attenuation in optical fibers could be less than $20 \mathrm{~dB} / \mathrm{km}$, optical fiber might be a suitable trans-
mission medium for light. They also suggested that the high losses of more than 1000 $\mathrm{dB} / \mathrm{km}$ were the result of impurities in the glass, not of the glass itself. By reducing these impurities low-loss fibers suited for communications would be produced. Within a few years of the Kao and Hockham's paper, Dr. Robert Maurer et. al., developed the fiber with losses less than $20 \mathrm{~dB} / \mathrm{km}$ in 1970 [20]. They manufactured a fiber with $17 \mathrm{~dB} / \mathrm{km}$ loss, by doping silica glass with titanium. Very soon in 1977 fibers were developed with theoretical minimum loss for silica-based fibers of $0.2 \mathrm{~dB} / \mathrm{km}$ at 1550 nm.

### 1.3 Evolution of Optical Communication

In the last century communication through electronic systems gained new heights and still providing technologically robust solutions. But as in the last decade, demand for more bandwidth has increased rapidly due to the data centric applications like internet TV, video on demand etc.. The two main hurdles in the scaling of the electronic systems are limited bandwidth of the communication medium and speed limitations of the electronic devices. To overcome these limitations optical communication was proposed. The foundation of optical communications was laid by the invention of the Laser in 1960. In 1966, basic structure and methodology of the optical fiber communication was proposed. The concept of optical communication gained new height with the inventions of the semiconductor laser and low loss fiber in the year 1970. By the end of year 1975, first continuous wave (CW) laser was invented. In the year 1980, American Telephone and Telegraph labs had set-up the first long haul system from Boston to Washington DC using graded index fiber. The first commercial 2G system at $1.3 \mu \mathrm{~m}$ wavelength through single mode fiber was implemented in 1982. One of the major break-through in optical


Figure 1.1: Schematic of first generation optical networks.
communication was the invention of Erbium-Doped Fiber Amplifier (EDFA) in 1987 by Pyne. In the year 1991, optical components like ( $\mathrm{LiNbO}_{3}$ modulators, arrayed waveguide gratings (AWGs) were commercialized. In 1996, first commercial WDM system was launched due to the commercial availability of WDM optical components. In the year 1998, intelligent WDM optical networking was initiated by Sycamore. In the year 2000, the concept of all-optical switching was demonstrated. Optical communication is still growing with the advent of new inventions.

### 1.4 Optical Networks

The development of optical communication networks took place in different steps and therefore they are classified as First, Second and Third Generation Networks [38, 48].

### 1.4.1 First Generation Optical Networks

The first generation of optical networks only provides point-to-point connectivity. This link can be static or manually configured (Figure 1.1) [21]. The technical issues involve in the first generation WDM network include the design and development of WDM lasers and optical amplifiers.


Figure 1.2: Schematic of second generation optical networks.

### 1.4.2 Second Generation Optical Networks

The second generation optical networks are capable of establishing connection-oriented end-to-end light paths by using optical add/drop elements (WADM/OADM) and optical cross connects. In the Figure 1.2, it is shown that the wavelength $W_{0}$ can be added/dropped form the network through optical add/drop multiplexes (OADM). The ring and mesh topology can be implemented using OADM and optical cross-connects (OXCs). The issues involved in the second generation optical network include the development of OADM, OXC, wavelength conversion, routing and wavelength assignment etc.

### 1.4.3 Third Generation Optical Networks

The third generation optical network is expected to support connection-less optical networking (Figure 1.3). Here, any input can be connected to any output by configuring the correct state of optical switch. The key issues include the development of passive optical network that can support optical $X$ switch (OXS) where $X=P$ (for packet), $B$


Figure 1.3: Schematic of third generation optical networks.
(for burst), $L$ (for level) and $C$ (for circuit) etc..
The different generation of the optical networks evolved over the years are summarized in Figure 1.4. Here, with the time the routing and signalling has moved from static to dynamic configuration and the traffic granularity which include volume as well as size of each traffic unit has moved form large to small. The switching paradigms properly investigated are optical $X$ switching (OXS) where $X$ can be $L, B$ and $P$ (level, burst and packet).

### 1.4.4 Structure of Optical Packet Switched Networks

In the next technological advancement, it is believed that edge router will remain in the electronic domain because of the advent of the CMOS technology (which allows data rate upto 40 Gbps ) and core routers will be implemented optically [65, 73]. This hybrid approach allows the efficient utilization of the mature electronic technology and huge bandwidth of the fiber in optical domain. The generic layout of the network is shown in Figure 1.5. The network structure is composed of core and client networks. The edge routers act as an interface between clients and core network. These edge routers


Figure 1.4: Evolution of the optical networks over the years.


Figure 1.5: Schematic of the generalized optical networks.


Figure 1.6: Schematic of the aggregated core networks.
lie on the periphery of the network cloud. In the current approach core as well as edge routers are assumed to be electronic in nature, but electronic switches/routers have speed limitations. Therefore, it is not possible to handle high data rate with electronic routers. The inefficiency of the electronic routers gave rise to birth of aggregated core optical networks. Since the data is generated by the electronic sources, only motivation to build the optical packet switch is when ingress node (edge router) aggregate the large number of packets optically for a very high bit rate payload. This can be attached with a low bit rate header and pushed into core network. The switch in the core network will convert the header of the packet in electronic domain and maintains the payload in optical form. The information stored in the header can be used to route the packet. As soon as packet reaches the egress node (edge router at which packet exits the core network), the aggregated packet can be separated optically and passed onto the client network. This type of networking structure is referred as aggregate core transport networks (Figure 1.6).

Therefore, one of the key issues involved in the optical networking is the design of the switch/router architecture which can performs switching operation efficiently at the high data rates. These can be classified as 'all'- optical or photonic switches. In alloptical mode data propagation and processing of the data is assumed to be in optical
domain. Currently, because of unavailability of the optical RAMs, all-optical switches are not technologically feasible. In the second mode (photonic) data remains in the optical domain without going through any $\mathrm{O} / \mathrm{E}$ and $\mathrm{E} / \mathrm{O}$ conversion at the intermediate nodes but control operation is performed in electronic domain. Still the photonic packet switching can provides high speed, format transparency and flexibility in the configuration due to the switching operation at physical layer.

### 1.5 Packet Switching

The concept of packet switching was first explored by Paul Baran in the early 1960 during his research on communication network at the RAND corporation for the US Air Force. Packet switching is a communication paradigm in which information is transmitted in the form of packets. These, packets are discrete blocks of data that are routed between nodes over the data links. In each network node, packets can be queued (buffered) or transmitted to output and it results in variable queuing delay. This is in contrast with circuit switching where path are established in advance and maintained till communication takes place. Packet switching technology is used to optimally utilize the channel capacity available in a network while maintaining the transmission latency (i.e. time taken by data to pass through the network) and increasing the robustness of networks. Packet switching does statistical multiplexing with very fine granularity [44]. In optical packet switching technology data in the packet is kept in optical domain without $\mathrm{O} / \mathrm{E}$ and $\mathrm{E} / \mathrm{O}$ conversion at switching nodes. The major issue involved in the optical packet switching is the architecture of the switch/router which can perform switching of the data efficiently while minimizing the buffering requirements. In this thesis, various optical packet switch architectures have been proposed along-with


Figure 1.7: Generic layout of photonic packet switch.
their detailed description, advantages and limitations. Their performance has also been evaluated at physical as well as network layer.

### 1.6 Photonic Packet Switching

Figure 1.7 shows the schematic diagram of a generic photonic packet switch. The key functions $[32,66]$ affecting the operation and implementation of a switch are:

1. Control,
2. Packet routing,
3. Packet synchronization,
4. Contention resolution, and
5. Packet header replacement.

### 1.6.1 Control

The main function of control units is to search routing database, decide the outgoing port and then configure various components of the switch such that packet can be directed to designated output port at a scheduled time.

### 1.6.2 Routing, Forwarding and Switching

Routing is distributed or centralized algorithm which results in routing table at each switch. Routing may be centralized or distributed. In centralized control, a single processor monitors the network and set-up the correct switching states as per the routing request. But, as the networks become larger or incorporate more and more switches, centralized control increases latency, degrades throughput, and also increases processing complexity. While in distributed control, the information carried by the packets is independently processed at each node. This form of processing reduces the burden on a centralized processor and increases the switch/network throughput. Additionally, the distributed routing decisions are based on local information, whereas the centralized routing decision are made on global and perhaps on the obsolete information. Hybrid of centralized and distributed routing control may provide optimal performance by combining advantages of both the techniques. Forwarding is a mechanism by which next suitable output is chosen which will guide the packet to its destination by searching the routing table [69]. Switching is the mechanism which configure state/path of the switches to facilitate the transfer of packet to the chosen output port.

### 1.6.3 Synchronization

Synchronization is a fundamental issue that must be taken into consideration when individual photonic switches are combined into a centralized or distributed switching networks [16]. In order to perform successful routing, the proper alignment of packets within the switch fabric and that of headers within the routing control processor is necessary. In general, optical packet switched networks can be divided into two categories based on synchronization: slotted (synchronous) and un-slotted (asynchronous). Since the state of switch fabric can only be changed at discrete times, it is crucial for the network designer to decide whether (or not) to have all the input packets aligned before they enter the switch fabric. In both these cases, bit-level synchronization and fast clock recovery are required for packet header recognition and packet delineation. In a slotted network, all the packets have same size. They are combined together with the header to form a fixed time slot. The duration of the slot is kept longer than the total duration of packet. This provides sufficient guard band between neighboring packets. In most cases, optical buffering is implemented by using fiber loops or delay lines with a propagation delay either equal to or a multiple of the time slot duration. This leads to the requirement that all packets arriving at the input ports should have the same size and be aligned in time slot boundary with local clock reference. In an un-slotted network, arriving packets may or may not have the same size. Packets arrive and enter the switch without being frame aligned. Here, the chance of contention is more because the behavior of incoming packets will be more unpredictable and less regulated. The buffering in optical domain in these networks is much more complex [70]. On the other hand, these switching networks will be more robust and flexible than the slotted networks. With careful design of node architecture and protocols according to the network specifications, satisfactory performance can be achieved even in un-slotted systems.

### 1.6.4 Contention Resolution

At the input of a switch, it is possible to receive more than one packets which need to be forwarded to same output port. Since only one packet can be transmitted to an output port at a given time, contention occurs. For the contention resolution, three solutions ([71],) are possible:

1. Deflection Routing in space domain,
2. Wavelength Conversion of the data in wavelength domain and
3. Optical Buffering in time domain.

Each of these methods has its own advantages and disadvantages. Wavelength conversion is easiest to implement, but the cost of the wavelength converters is a major issue. Deflection routing is cost effective as it does not require any additional hardware. But in this process, latency is higher resulting in less throughput. Optical buffering provides solution with low latency at moderate cost. Thus, using these methods separately or in combination can achieve higher throughput and efficiency in the switching network. Buffering switches can block, drop or deflect the packet to control traffic flow and resolve contention. In this thesis, combination of both wavelength conversion and optical buffering have been considered.

### 1.6.4.1 Deflection Routing

In deflection routing, contending packets are routed and forwarded to some other link. Routing decisions for deflection of packets are based on destination address and packet priorities. Deflection routing techniques require that the network topology should be
multi-path or re-circulatory, so that the deflected packets can be routed to the destination following an alternate path. The priority of deflected packet is increased to reduce the end-to-end latency and to avoid deflecting a packet indefinitely.

### 1.6.4.2 Wavelength Conversion

In wavelength conversion packets are routed on the same/different link on a different wavelength. The wavelength conversion is more effective when it is used in combination with buffering/deflection routing. Wavelength conversion had been shown to reduce the number of optical buffers and also the packet loss probability [12].

### 1.6.4.3 Buffering



Figure 1.8: Schematic of traveling type buffer structure.

When data packet reaches a node, it has to be stored till control module decides on which path this packet has to be forwarded. Once the decision has been made


Figure 1.9: Schematic of re-circulating type buffer structure.
about the packet's routing, packet is retrieved from the delay lines and forwarded to output port as per the decision. Advanced electronic RAMs can be used for packet buffering however electronic RAMs have a limited access speed, which will eventually constrain the speed and capacity of photonic packet switching system. In addition, this approach requires optical to electrical ( $\mathrm{O} / \mathrm{E}$ ) conversion and vice-versa when packets are written into and read out from the electronic RAMs, adding to the complexity. All-optical RAM suitable for photonic packet switching has not been developed. Optical fiber delay lines can be used by incorporating components such as optical gate switches, optical couplers, optical amplifiers, and wavelength converters to realize photonic buffering. A number of photonic packet buffers based on optical fiber delay lines have been proposed and demonstrated all across the world [66]. In general these optical fiber delay lines based buffers can be classified into two basic categories: traveling-type and re-circulating type. A traveling-type buffer generally consist of multiple optical fiber delay-lines whose lengths are equivalent to multiples of a packet duration $T$, and optical switches to select delay lines (Figure 1.8) [25]. The re-circulating type buffer is more flexible than the traveling type buffer because the packet storage time can be adjusted by changing the number of re-circulations (Figure 1.9) [18]. In principle recirculating type buffer offer a kind of random access where storage time depends on the number of re-circulations. In the recent past, slow light based buffering techniques have been proposed and demonstrated, but currently they are not considered as viable option due to large attenuation loss [6]. The optical buffering can be performed at the input, output and in shared manner in the switch fabric [24]. In these techniques generally input buffering is not preferred, while other two are more frequently used in the switches.

### 1.6.4.4 Input Buffering



Figure 1.10: Schematic of input buffering scheme.

In input buffering scheme (Figure 1.10), a separate buffer is placed at each input of the switch and each arriving packets momentarily enter into the buffering unit. If buffer is vacant, output port is free and in the other buffers (buffer available at other inputs) there is no packet for that particular output, then arriving packet will be forwarded to the appropriate output and if buffer is not empty then it will be placed in the buffer and will leave the buffer such that FIFO can be maintained for each output ports. In the input queuing, head of line blocking occurs and maximum possible throughput is only 0.586 [24].

### 1.6.4.5 Output Buffering

In output buffering scheme (Figure 1.11), a separate buffer is placed at the each output port of the switch and arriving packets are transferred to appropriate output port and will be processed such that FIFO can be maintained. In the output queuing structure no internal blocking occurs and hence large throughput is achievable. In output buffered switches speed-up factor of $N$ is required for $N \times N$ switch.


Figure 1.11: Schematic of output buffering scheme.

### 1.6.4.6 Shared Buffering



Figure 1.12: Schematic of shared buffering scheme.

The above discussed input/output buffering schemes are not cost effective because at each port of the switch a separate buffer is required. Therefore, hardware complexity is very large. In the shared buffering scheme (Figure 1.12) contending packets for all the outputs are stored in the common shared buffer. Therefore, hardware complexity is less and still higher throughput is achievable [2].

## G. B. = Guard Band



Figure 1.13: Schematic of the packet format.

### 1.6.5 Packet Header Replacement

Header regeneration involves computing, generating and re-inserting a header with the associated payload before it leaves from the appropriate switch output port. There are several circumstances where this functionality is required e.g., in an all-optical photonic packet switch where the header is completely removed from the payload for processing, or where the routing strategies requires a modification of the packet header. It is important that the header regeneration technique should be able to operate for cascaded switches and independent of the number of switches, the packet traverses.

### 1.6.5.1 Header and Packet Format

A packet can be functionally described using a layered model. At the physical level, there are effectively two such layers: the header and the payload. The header contains information processed only by the switches. It may include destination address, priority, packet empty-full bit and packet length. The payload contains information processed only by the sources and destinations. It may include data, packet number and source address. As the header has to be processed at each switch node, it is desirable that the header has a relatively low fixed bit rates. The use of fixed length packets can simplify the implementation of packet contention resolution packet routing and packet synchronization. The packet switching does not require a link with a dedicated and reserved bandwidth. Depending on the network and on the available bandwidth on
different line any packets may take several possible routes to reach the destination. In such a case a sequence number is included in the packets to insure that the packets will not be misinterpreted if they arrive out of order. The size of the packets (fixed/variable) depends on the network design structure. For the simplification of the architecture, packets of equal length are considered in this thesis, and it is assumed that at each input, packets are synchronized. This synchronization can be achieved by using techniques discussed in [16]. In this thesis ATM like packet of fixed length of 55 bytes is assumed (Figure 1.13).

### 1.7 Switch Architectures

The design of optical switches/routers critically effects the performance of the networks. In past, different photonic packet switch architectures have been proposed and demonstrated. All these architectures use photonic means to perform packet buffering and routing; electronics plays the important role in functions such as address processing, routing and buffering control. Optical packet switch architectures in broad sense can be classified into three categories:

1. Wavelength routed photonic packet switch
2. Broadcast and select type switch
3. (AWG)/Space switch based packet switch

### 1.7.1 Wavelength Routed Photonic Packet Switch

In this class of switches, wavelength coding is used for buffering and routing of packets. The switch consists of three functional blocks: a packet encoder block, a buffering block and packet de-multiplexer block. The encoder block encode the wavelengths of the incoming packets, buffering block buffer the encoded packets if necessary and demultiplexer block separate the packets and direct them to the appropriate output ports $[13,22,23,27,57,66,76,77]$.

### 1.7.2 Broadcast and Select type Switch

In this approach, at the input of the switch all the information is multiplexed by a star coupler, and distributed to all the outputs. Each receiver at the output selects a particular packet only. Both time division multiplexing (TDM) and wavelength division multiplexing (WDM) can be used in these switches. In this category, contending packets are stored in fiber delay lines using WDM technology. The various loop buffer based architectures can be found in $[4,11,18,42,50,51,52,53,59,64,67]$. All of them have their advantages and disadvantages which are well described in their respective references.

### 1.7.3 AWG/Space Switch based Architectures

The third class of architecture uses AWG/Space Switch as a router. The insertion loss of the AWG router is less as compared to splitter and combiner. Thus using AWG, comparatively large number of users can be accommodated. The various AWG/Space switch based architectures can be found in $[10,36,45,58]$. In broad sense, these
architecture performs better than the re-circulating type loop buffer architecture. In this thesis, various optical packet switch architectures have been presented. The architecture from A1 to A7 (nomenclature of the architectures considered in the thesis) are broadcast and select type in nature whereas, architecture A8 is AWG based architecture.

### 1.8 Switch Design Considerations

In optical packet switch design, several key factors need to be considered. The key parameters that would influence the design of a DWDM packet switching system are described in next sub-sections [34].

### 1.8.1 Nominal Central Frequency

International Telecommunication Union (ITU)-T band recommends nominal central frequencies or wavelengths for a specific band of operation, for example, in $C$ band 193.1 THz is a reference frequency and all other frequencies are calculated as $F=$ $(193.1+m \Delta \nu) \mathrm{THz}$ where $m$ is an integer and $\Delta \nu$ inter channel spacing in GHz [34]. One should note that attenuation is minimum in this window (region around 193.1 THz).

### 1.8.2 Channel Spacing

Channel spacing is the difference of wavelength or frequency between adjacent channels in WDM system. The channel spacing critically effects the performance of the switch because smaller channel spacing can accommodate more number of channels but intersymbol interference (ISI) will be large. WDM systems are classified based on channel
spacing as follows:

1. Coarse WDM (CWDM) - channel spacing $<50 \mathrm{~nm}$,
2. Wide WDM (WWDM) - channel spacing $>50 \mathrm{~nm}$ and
3. Dense WDM (DWDM) - channel spacing $=0.8 \mathrm{~nm}$.

### 1.8.3 Channel Capacity

Channel capacity is the maximum number of channels on which switch or photonic component can operate. This limit is not because of transmission medium, but due to the transmission impairments and allowed range of components.

### 1.8.4 Channel Bit Rate

Channel bit rate is the maximum bit rate on which a switch or photonic components can operate properly. This bit rate will be the deciding factor for switching speed and operating time for all the photonic components.

### 1.8.5 Channel Performance

The channel performance is measured in term of bit-error rate (BER). This will have impact on allowable degradation in the switch hence its throughput performance.

### 1.8.6 Maximum Buffering Time

Maximum buffer time is the maximum duration for which a packet can remain in buffer and then received correctly at the output. Buffering time will be decided by the maximum number of re-circulations (in case of recirculating type buffer) that a packet can take at specified BER. If a packet is stored for more than this limit, it will become unusable due to accumulated noise and transmission impairments.

### 1.8.7 Optical Power Budget

The optical power budget is the calculation of all the signal losses at every component e.g., coupler, optical mux, demux, TWC, optical fibre, splices, connectors, etc. in the optical path between a transmitter and receiver. The main objective is to ensure that the power of optical signal at the receiver is greater than the minimum detectable optical power (receiver sensitivity). For WDM systems power budget for each wavelength is evaluated separately.

### 1.8.8 Transmission Impairments

### 1.8.8.1 Attenuation in Fiber

Attenuation is the loss in signal power as it propagates through the fiber. The attenuation loss is generally caused by the material absorption and Rayleigh scattering in optical fiber. The attenuation of an optical fiber depends on the wavelength on which transmission is made. There are two commonly used wavelengths i.e., 1310 and 1550 nm . The minimum attenuation occurs at 1550 nm and is approximately $0.2 \mathrm{~dB} / \mathrm{km}$ (Figure 1.14), while dispersion is at minimum at 1310 nm . The maximum number of


Figure 1.14: Attenuation curve of the fiber with respect to wavelengths.
allowed channels at different band at different bit rate and channel spacing is shown in Table 1.1.

| Colour | Band | Wavelength Range | Channels <br> at 10 Gbps <br> Spacing 100 GHz | Channels <br> at 2.5 Gbps <br> Spacing 50 GHz |
| :---: | :---: | :---: | :---: | :---: |
| Sky blue | C band | $1530-1560 \mathrm{~nm}$ | 40 | 96 |
| Purple | L band | $1560-1600 \mathrm{~nm}$ | 40 | 100 |
| Brown | S band | $1480-1520 \mathrm{~nm}$ | 40 | 100 |

Table 1.1: Channels allocation at different band at different bit rate and channel spacing

### 1.8.8.2 Crosstalk

This effect occurs basically because of energy leakage from other co-propagating signals to the optical signal of interest due to the non-ideal optical devices. Almost every component including wavelength multiplexers/de-multiplexes and fiber itself introduce crosstalk between different wavelength channels. Crosstalk is an undesirable effect and should be as small as possible.


Figure 1.15: Schematic of the ISI between adjacent channels.

### 1.8.8.3 Channel Dispersion

Dispersion refers to a phenomenon in which a signal pulse spreads out in time as it propagates through a fiber. When pulse spreads it overlaps with neighboring pulses and inter-symbol interference happens between the neighboring pulses (Figure 1.15). This constraint imposes limit on the minimum possible separation between the pulses and the maximum possible bit rates. The simplified bit rate and dispersion relation to keep ISI within limit is given by [6],

$$
\begin{equation*}
B_{R} L|D| \Delta \lambda<1 \tag{1.8.1}
\end{equation*}
$$

where $B_{R}$ is the bit rate, $L$ is the transmission length, $|D|$ is dispersion coefficient and $\Delta \lambda$ is the source spectral width.

### 1.8.8.4 Non-Linear Effects

As the power of the signal propagating through the fiber increases the non-linear effects start to dominate. Non-linear effects in fiber may leads to signal attenuation, distortion, interference and therefore have significant effects on the performance of the WDM transmission systems. There are number of nonlinear effects including self-phase modulation (SPM), cross-phase modulations (XPM), stimulated Raman scattering (SRS),


Figure 1.16: Non-linear effects vs. bit rate per channel.
stimulated Brillouin scattering (SBS) and four-wave mixing (FWM) [9] which can occur in fiber. These effects impose limits on the spacing between two optical channels, maximum power of the signal and maximum transmission rate. In WDM systems, FWM have detrimental effects (Figure 1.16) [31]. It has been described in chapter 3.

### 1.9 Wavelength Management

The signal integrity on a wavelengths assigned in WDM system should be continuously monitored. Management includes locating fault and isolation of all the faulty components. When a signal quality degrades on a channel, then wavelength management should be able to dynamically assign another wavelength or drop the packet in case it integrity cannot be maintained.

## Wavelength Selection and Spacing

Wavelength selections is an important criterion and should be done considering the following parameters:

1. Crosstalk minimization,
2. Minimization of four wave mixing degradation,
3. Dispersion minimization and
4. Equal gain for each wavelength.

The first and third point demands that frequency spacing should be as large as possible so that high data rate can be supported; the second point demands that channel spacing should be unequal and the last point demands that frequency spacing should be kept as small as possible.

### 1.10 Fiber Selection

Optical fibers are classified as single and multi-mode fibers. At very high data rates, single mode fiber is employed. These can be further divided into three types.

### 1.10.1 Standard Single Mode Fiber

This fiber was designed to provide zero chromatic dispersion at 1310 nm to support the early long haul transmission systems operating at this wavelength.

### 1.10.2 Dispersion Shifted Fiber

The attenuation of the fiber is minimum at $1550 \mathrm{~nm}(0.2 \mathrm{~dB} / \mathrm{km})$. To operate at lowest loss, dispersion shifted fiber have been designed which has zero dispersion at 1550 nm
instead of 1310 nm . But the detrimental effect of FWM is more pronounced at zero dispersion.

### 1.10.3 Non Zero Dispersion Shifted Fiber

Although DSF fiber overcome the problems of chromatic dispersion at 1550 nm but the problem of four wave mixing starts to dominate in WDM networks. To overcome this, NDF was developed. In these fibers very little dispersion is intentionally provided to minimize the harmful effect of FWM.

### 1.10.4 Operation Window

The operation window of the optical communication depends on number of factors. There are number of impairments which pushes the switch operation in narrow region. The operation window start to shrink as any one of the above mentioned effects starts to dominate. For example, as the number of channels increases the total power propagating through the fiber increases and due to the non-linear effect, window start to shrink (Figure 1.17). The window sizing under different constraints will be explored in Chapter 3.

### 1.11 Different Components in Optical Switch

### 1.11.1 3 dB Coupler

An optical fiber coupler is a device that distributes light from a main fiber into one or more branch fibers. Light from the input fiber is coupled to the output fiber according


Figure 1.17: Schematic of the shrinking window.


Figure 1.18: Schematic of $2 \times 2$ coupler.
to the degree of overlap. Hence, the input power can be distributed in a well-defined proportion by appropriate control of the amount of lateral offset between the fibers. Couplers are passive and bi-directional devices. A simple configuration is $2 \times 2$ coupler as shwon in Figure 1.18. In $2 \times 2$ coupler light can be coupled in different proportions; if in one fiber it is $\alpha$ then in other, it is $1-\alpha$ where $\alpha$ is a fractional number between 0 and 1.

The transfer function of a $2 \times 2$ coupler can be written as

$$
\left[\begin{array}{c}
E_{\text {out }}(1)  \tag{1.11.2}\\
E_{\text {out }}(2)
\end{array}\right]=\left[\begin{array}{cc}
\sqrt{\alpha} & j \sqrt{1-\alpha} \\
j \sqrt{1-\alpha} & \sqrt{\alpha}
\end{array}\right]\left[\begin{array}{c}
E_{\text {in }}(1) \\
E_{\text {in }}(2)
\end{array}\right]
$$

For the coupling coefficient of $\alpha=0.5$ the coupler is referred as 3 dB coupler.
Assuming that the power which is square of the electric field entering through the input port 1 is $P_{\text {in }}(1)$ and from the port 2 it is zero. The power at the output port 1 and 2 is $P_{\text {out }}(1)$ and $P_{\text {out }}(2)$ respectively. The important loss parameters of the coupler are as follows

$$
\begin{equation*}
\text { Excess Loss }=P_{\text {out }}(1)+P_{\text {out }}(2)-P_{\text {in }}(1) \tag{1.11.3}
\end{equation*}
$$

when $P_{\text {in }}(2)=0$.
The excess loss defines the light absorbed by the device.

$$
\begin{equation*}
\text { Insertion Loss }=P_{\text {out }}(1)-P_{\text {in }}(1) \tag{1.11.4}
\end{equation*}
$$

Usually, power loss due to the insertion loss is the sum of power lost due to the split loss and power lost due to excess loss. In WDM coupler another important factor is isolation. Isolation means how much unwanted light is reached at the output ports. This is undesired effect, so isolation should be as large as possible (typically 40 to 50 dB)

### 1.11.2 Splitter and Combiner



Figure 1.19: Schematic of splitter and combiner.


Figure 1.20: Schematic of mux and demux.

Splitter is a device that divides the power of the incoming signals in equal parts and combiner does the opposite. These are wavelength in-sensitive devices. Therefore, power of all the signals arriving at different wavelengths on each input appears at all the output ports of the splitter. Schematic of a $1 \times N$ ports splitter and a $N \times 1$ combiner are shown in Figure 1.19. The power appearing at each output ports will be $1 / N$ part of the incoming power. The insertion loss of the devices is large and approximately equal to $\left(10 \log _{10} N\right)$. These devices are generally used for the broadcasting of optical signals.

### 1.11.3 Multiplexer and De-multiplexes

Multiplexes/De-multiplexes are the optical devices that combine and separate light signals at different wavelengths (Figure 1.20). These devices are wavelength sensitive and reciprocal in nature. WDM mux/demux are generally based on array waveguide grating or interferometric principles. The number of channels (or number of wavelengths) that can be multiplexed/de-multiplexed are typically multiple of two e.g., 4, 8, 16, 32 etc.

### 1.11.4 Arrayed Waveguide Gratings

An arrayed waveguide grating consist of input and output slab waveguide based multiport couplers and in between an array of fiber where length of each fiber differ by


Figure 1.21: Schematic of array waveguide grating.

| Routing <br> Pattern |  | Out puts |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | 1 | 2 | 3 | 4 |
| $\begin{aligned} & \text { 号 } \\ & \text { 首 } \end{aligned}$ | 1 | $\lambda_{1}$ | $\lambda_{2}$ | ${ }_{3}$ | $\lambda_{4}$ |
|  | 2 | $\lambda_{2}$ | ${ }^{\prime}$ | $\lambda_{4}$ | $\lambda_{1}$ |
|  | 3 | $\lambda_{3}$ | $\lambda_{4}$ | $\lambda_{1}$ | $\lambda_{2}$ |
|  | 4 | $\lambda_{4}$ | $\lambda_{1}$ | $\lambda_{2}$ | ${ }_{3}$ |

Figure 1.22: Schematic of routing pattern of $4 \times 4$ AWG
some fixed length $\Delta L$. The arrayed waveguide gratings works on the phenomenon of interferometry. These are commonly used as optical multiplexers/de-multiplexes in wavelength division multiplexed (WDM) optical systems (Figure 1.21). The arrayed waveguide gratings follow a specific routing pattern for different wavelengths. The routing pattern of $4 \times 4 \mathrm{AWG}$ is shown in Figure 1.22.

### 1.11.5 Filters (TF/FF)

Optical filters are the devices which either select or reject wavelengths. Optical filters are based on the principal of interferometry and are classified as fixed (FF) and tunable filters (TF). Fixed filters always select a particular wavelength and in contrast to this tunable filters can be tuned to any wavelength in the allowed range of the filter. In fixed filters category, generally fabry-perot and thin film based filters are used in optical
domain. The dielectric thin film based stack can also be used as reflector. The tuning of the filters can be done using mechanical stress, acousto-optic and electro-optic phenomenon. In optical packet switching electro-optical filters are preferred over others due to the fast switching time ( $\sim$ ns $)$. The main requirements of the optical filters are:

1. Fast switching time,
2. Wide tuning range,
3. Flat top pass band and
4. Narrow bandwidth.

### 1.11.6 Optical Cross Connects (OXCs)

Optical cross connect, switch the data from one input port to any one of the output ports. OXCs are wavelength insensitive device. Therefore any input can be routed to any output by configuring the OXCs. Generally they are developed using array of SOAs. Therefore switching speed of the order of few $\sim \mathrm{ns}$ is feasible.

### 1.11.7 Tunable Wavelength Converters



Figure 1.23: Schematic of the tunable wavelength converter.

A wavelength converter is a device that is capable of converting one wavelength (a set of wavelengths) to another wavelength (other set of wavelengths) (Figure 1.23). In general a wavelength converter is expected to have following characteristics [34]

1. Transparency to bit rates and signal formats,
2. Different wavelength conversion capability,
3. Large conversion range,
4. Fast tuning time,
5. Polarization independence,
6. Large signal - to - noise ratio and
7. Easy implementation.

In optical packet switching generally variable input-variable output converters are desirable, so that any incoming wavelength can be converted to any outgoing wavelength.

### 1.11.8 Isolators and Circulators



Figure 1.24: Schematic of the isolator.

An isolator is a device, which allows transmission in one direction through it, but blocks all transmission in other direction (Figure 1.24). Isolators are used in front of optical amplifiers and lasers primarily to prevent reflections from entering these devices, which would otherwise degrade their performance. The two key parameters of isolators


Figure 1.25: Schematic of the circulator.
are the insertion loss which is the loss in forward direction, which should be as small as possible and its isolation which is the loss in the reverse direction and should be as large as possible. The typical insertion loss is 0.15 dB and the isolation is around 50-60 dB [34]. The circulators are the isolators with more than two ports. In the circulators also the signal flows in one direction only. In the networks/switch circulators are used to add/drop the signals as shown in the Figure 1.25. Here it is shown that with the use of fiber Bragg grating wavelength $\lambda_{3}$ is dropped at the port 3 of the circulator.

### 1.11.9 Fiber Bragg Gratings

Fiber Bragg grating is a device which reflect a particular wavelength or set of wavelengths while transmit the remaining ones. This is achieved by the periodic perturbation of refractive index of the core of the fiber. Therefore, this device acts as optical filter. The reflected wavelength $\lambda_{B}$, called the Bragg wavelength, is defined by the relationship,

$$
\begin{equation*}
\lambda_{B}=2 n \Lambda \tag{1.11.5}
\end{equation*}
$$

where, $n$ is the effective refractive index of the grating in the fiber core and $\Lambda$ is the grating period. Using chirp fiber gratings, a set of wavelengths can be reflected by a single gratings. In chirp gratings refractive index profile of the grating is modified which varies the grating period linearly or in desired manner as per the design.

### 1.11.10 Transmitters

An optical transmitter is a system with light source that generates an optical signal at particular wavelength, which is modulated by an electrical signal and can be classified into two categories: LASERs (Light Amplification by Stimulated Emission and Radiations) and LEDs (Light Emitting Diodes). Lasers are used for long distance transmissions and LEDs for short distance transmissions. As per the transmission requirements both fixed or tunable lasers can be used.

### 1.11.11 Receivers



Figure 1.26: Schematic of the receiver.

An optical receiver is a device that converts an optical signal to the electronic data signal at the output. It consist of four functional blocks: a pre-amplifier, a photo- detector, a front end amplifier and a recovery circuit (Figure 1.26) [34]. The pre-amplifier boosts the incoming signal. The photo-detector generates an electrical current called photocurrent, proportional to the incoming optical power. The front-end amplifier increases the level of electrical current. To recover transmitted bits at the receiver, the receiver circuit performs clock recovery, sampling, and detection with respect to an estimated threshold.

### 1.11.12 Optical Amplifiers

### 1.11.12.1 Semiconductor Optical Amplifiers

Semiconductor optical amplifier are used for amplification of the optical signal. The main advantage of SOA is its compact size. Consequently can be easily integrated with other optical components. SOAs also have switching speed of the order of few ns. In some applications SOA can also be used as gate switch. The disadvantage associated with SOAs are:

1. Polarization dependence,
2. Introduces cross-talk,
3. Bit rate format dependency and
4. High noise figure.

### 1.11.12.2 Erbium Doped Fiber Amplifiers



Figure 1.27: Schematic diagram of the EDFA.

The advent of Erbium Doped Fiber Amplifier (EDFA) was a major breakthrough in optical communication. The EDFA, like SOA amplifies the incoming signal in optical domain. Therefore, expensive $\mathrm{O} / \mathrm{E}$ and $\mathrm{E} / \mathrm{O}$ conversions is not needed. An EDFA
consists of a piece of fiber, whose core is uniformly doped with Erbium ions (Figure 1.27). A strong beam of laser light at the proper wavelength ( 980 nm or 1480 nm ) known as pump is propagated into the core of the fiber in order to excite Erbium ions creating population inversion. As a result, stimulated emission can produce amplified light at the output of the amplifier. In addition to this, spontaneous emission also exist and leads to the amplified spontaneous emission (ASE) noise of the amplifier. The ASE noise power spectral density is given by [48],

$$
\begin{equation*}
S_{A S E}=n_{s p}(G-1) h \nu \quad \text { Watts } / \mathrm{Hz} \tag{1.11.6}
\end{equation*}
$$

Here,
$\mathrm{G}=$ Gain of amplifier,
$\nu=$ Signal frequency,
$n_{s p}=$ Population inversion factor of the optical amplifier and $h=$ Planck constant .

## Advantages of EDFA

1. Commercially available in C band (1530 to 1565 ) and L band (1560 to 1605).
2. Excellent coupling.
3. Insensitivity to light polarization state.
4. Low sensitivity to temperature.
5. High gain.
6. Low noise figure.
7. No distortion at high bit rate.
8. Simultaneous amplification of WDM signals.
9. Immunity to cross talk in wavelength multiplexed channels.

## Drawbacks of EDFA

1. Pump laser is necessary.
2. Difficult to integrate with other components.
3. Need gain equalization for multistage amplification.
4. Dynamic control is necessary.

### 1.12 Noise Sources

In optical communication in addition to optical amplifier noise, there are other noise sources which also degrade the system performance.

### 1.12.1 Shot Noise

Ideally input power arriving form the source is constant, which means that the number of photons per unit of time, on an average is constant. But in real scenario, actual number of photons arriving at a particular time is unknown and is a random variable. Additionally the number of electrons producing photocurrent will also vary because of their random re-combinations and absorptions. Therefore, even though the average number of electrons is constant, the actual number of electrons will vary. Deviation of
actual number of electrons from the average number is known as shot noise [48]. The spectral density of the shot noise is given by

$$
\begin{equation*}
S_{s}=2 q I \quad \text { Watts } / \mathrm{Hz} \tag{1.12.7}
\end{equation*}
$$

The variance of random variable added to sampled signal value will be given by

$$
\begin{array}{r}
\sigma_{s}^{2}=2 q I B_{e} \\
\text { where } \quad I=R P \tag{1.12.9}
\end{array}
$$

where, $q$ is the electronic charge, $R$ is the responsivity of the photodiode, $P$ is the optical power of the incoming signal and $B_{e}$ is the electrical bandwidth of the receiver. Shot noise is assumed to be white noise and hence its spectral density is independent of frequency.

### 1.12.2 Thermal Noise

Electron motion due to temperature variation occurs in a random manner. Thus, the number of electrons flowing through a given circuit at any instance is a random variable. The deviation of an instantaneous number of electrons from their average value because of temperature is called thermal noise [48]. Double sided spectral density of the thermal noise is given by

$$
\begin{equation*}
S_{T}=\frac{2 K_{B} T}{R_{L}} \tag{1.12.10}
\end{equation*}
$$

Thus the variance of noises added to the sampled signal value is,

$$
\begin{equation*}
\sigma_{T}^{2}=\frac{4 K_{B} T B_{e}}{R_{L}} \tag{1.12.11}
\end{equation*}
$$

In the above expressions, $K_{B}$ is Boltzmann constant, $T$ is the temperature and $R_{L}$ is the load resistance.

### 1.12.3 Beat Noise

Photo-detector is a square law device which responds to the intensity (i.e. proportional to square of the incoming electric field) of the incoming signals. Therefore, different beat noise terms are produced at the receiver. The different noises beating terms at the receiver are as follows [48],

The Shot noise

$$
\begin{equation*}
\sigma_{s}^{2}=2 q R P B_{e} \tag{1.12.12}
\end{equation*}
$$

The ASE -ASE beat noise

$$
\begin{equation*}
\sigma_{s p-s p}^{2}=2 R^{2} P_{s p}^{2}\left(2 B_{0}-B_{e}\right) \frac{B_{e}}{B_{0}^{2}} \tag{1.12.13}
\end{equation*}
$$

The Sig-ASE beat noise

$$
\begin{equation*}
\sigma_{s i g-s p}^{2}=4 R^{2} P P_{s p} \frac{B_{e}}{B_{0}} \tag{1.12.14}
\end{equation*}
$$

The Shot-ASE beat noise

$$
\begin{equation*}
\sigma_{s-s p}^{2}=2 q R P_{s p} B_{e} \tag{1.12.15}
\end{equation*}
$$

The Thermal noise will be given by.

$$
\begin{equation*}
\sigma_{t h}^{2}=\frac{4 K_{B} T B_{e}}{R_{L}} \tag{1.12.16}
\end{equation*}
$$

The expression for $P$ and $P_{s p}$ will be given by

$$
\begin{array}{r}
P=b P_{\text {in }} \\
P_{s p}=n_{s p}(G-1) h \nu B_{0} \tag{1.12.18}
\end{array}
$$

Here, $b P_{i n}$ is the power of incoming signal for bit $b$ and $B_{0}$ is the bandwidth of the optical filter.

### 1.13 Performance Evaluation Parameters

The performance evaluation of the switches can be done both at physical as well as at the network layer. In the physical layer, effects of system impairments on bit-error rate (BER) is discussed. The network layer performance of the switch is measured in terms of packet loss probability to observe the efficiency of the switch and low packet loss probability is desirable to achieve high throughput.

### 1.13.1 Bit Error Rate

The BER depends on the SNR of the current generated at the receiver when optical bit stream is converted into the electric domain. The SNR in turn depends on various noise mechanisms such as shot noise and ASE noise associated with the received signal. The fluctuating electric signal at the receiver is passed to the decision circuit which samples it periodically at the bit rate to determine individual bits. The sampled value $I$ fluctuates from bit to bit around an average value of $I_{1}$ or $I_{0}$ depending on whether the bit correspond to ' 1 ' or ' 0 ' in the pattern stream. The decision circuit compares the sampled value with a threshold value $I_{D}$ and calls it bit ' 1 ' if $I>I_{D}$ and bit ' 0 ' if
$I<I_{D}$. An error occurs if $I<I_{D}$ for bit ' 1 ' because of receiver noise. An error is also occurs if $I>I_{D}$ for bit ' 0 '. Both sources of errors can be included through the error probability defined as

$$
\begin{equation*}
B E R=P(1) P(0 / 1)+P(0) P(1 / 0) \tag{1.13.19}
\end{equation*}
$$

Here, $P(1)$ and $P(0)$ are the probabilities of receiving bit ' 1 ' and ' 0 ' respectively $P(0 / 1)$ is the conditional probability of deciding ' 0 ' when a ' 1 ' bit is received and $P(1 / 0)$ is the conditional probability of deciding ' 1 ' when a ' 0 ' bit is received. Since ' 1 ' and ' 0 ' bits are equally likely to occur in a realistic bit stream $P(1)=P(0)=1 / 2$ and the BER becomes

$$
\begin{equation*}
B E R=\frac{1}{2}[P(0 / 1)+P(1 / 0)] . \tag{1.13.20}
\end{equation*}
$$

The quantity $P(0 / 1)$ and $P(1 / 0)$ depends on the probability density function of the sampled value $I$. The functional form of $P(I)$ depends on the statistics of various noise sources responsible for current fluctuations. Considering that the $P(I)$ is random Gaussian process then

$$
\begin{equation*}
B E R=0.5 \operatorname{erfc} \frac{Q}{\sqrt{2}} \tag{1.13.21}
\end{equation*}
$$

Here,

$$
\begin{equation*}
Q=\left(\frac{I_{1}-I_{0}}{\sigma_{1}+\sigma_{0}}\right) . \tag{1.13.22}
\end{equation*}
$$

The expression for BER becomes [48]

$$
\begin{equation*}
B E R=0.5 \operatorname{erfc}\left(\frac{I_{1}-I_{0}}{\sqrt{2}\left(\sigma_{1}+\sigma_{0}\right)}\right) . \tag{1.13.23}
\end{equation*}
$$

In the above expression $I_{1}, I_{0}$ are photocurrent and $\sigma_{1}, \sigma_{0}$ are noise variances for bit ' 1 ' and ' 0 ' respectively.

### 1.13.2 Packet Loss Probability

The performance evaluation of the switches at the network layer is done in terms of packet loss probability. The packet loss probability also depends on the traffic statistics. In this thesis, for the performance evaluation two traffic models are considered.

## Random Traffic Model

The random traffic model is simple; still it provides good insight of the architecture. This model assumes that packet can arrives at any of the inputs with probability $p$ and each packet is equally likely to be destined to any one of the outputs with probability $1 / N$. Thus the probability that $K$ packets arrive for a particular output in any time slot is given by

$$
\begin{equation*}
P(K)={ }^{N} C_{K}\left(\frac{p}{N}\right)^{K}\left(1-\frac{p}{N}\right)^{N-K} \tag{1.13.24}
\end{equation*}
$$

## Bursty Traffic Model

In reality, data traffic is usually bursty in nature. In the bursty traffic, arrivals are correlated i.e., packets arrive in the form of bursts. It is characterized by the offered load $(\rho)$ and burst length $(B L)$ [23]. Each burst of packets is equally likely to be destined to any of the output with probability $1 / N$. This also implies that if a packet arrives on input $i$ and destined for the output $j$ in the current slot, then there is small but finite probability, that in the next slot, packet arrives for the same destination. Thus, in the time domain, traffic at each input is composed of burst of packets destined for the same


Figure 1.28: Markov chain model for the bursty traffic.
output. Time correlation of the traffic on each input is characterized by the Markov chain model. This model assumes three stages:

1. Idle state,
2. Burst I state and
3. Burst II state.

The system will be in idle state, if no packet arrives in current slot. If we consider that with probability $P_{a}$ no packet arrives in the next slot. Then burst will remain in the idle slot. Thus, with probability $\left(1-P_{a}\right)$ a new burst will start, and system will go in the burst state I. Now considering that with probability $P_{b}$ new burst will arrive for the same destination. The burst can terminate in two ways

1. A new burst start for another destination with probability $\left(1-P_{a}\right)\left(1-P_{b}\right)$,
2. by going to idle state with probability $\left(P_{a}\right)\left(1-P_{b}\right)$.

The steady state distribution of the Markov chain can be obtained as

$$
\begin{equation*}
\pi P=\pi \tag{1.13.25}
\end{equation*}
$$

Here $\pi$ is row vector $\pi=\left[\begin{array}{lll}\pi_{1} & \pi_{2} & \pi_{3}\end{array}\right]^{T}$ and $P$ is transition matrix

$$
\left[\begin{array}{ccc}
P_{a} & \left(1-P_{b}\right) P_{a} & \left(1-P_{b}\right) P_{a}  \tag{1.13.26}\\
\left(1-P_{a}\right) & P_{b} & \left(1-P_{a}\right)\left(1-P_{b}\right) \\
0 & \left(1-P_{a}\right)\left(1-P_{b}\right) & P_{b}
\end{array}\right]\left[\begin{array}{l}
\pi_{1} \\
\pi_{2} \\
\pi_{3}
\end{array}\right]=\left[\begin{array}{l}
\pi_{1} \\
\pi_{2} \\
\pi_{3}
\end{array}\right]
$$

with

$$
\begin{equation*}
\sum_{i=1}^{3} \pi_{i}=1 \tag{1.13.27}
\end{equation*}
$$

Here, all the burst state after idle are considered together as burst state - 1 and all the burst state after another burst state are considered together as state - 2. By solving equations 1.13.26 and 1.13.27 we get

$$
\begin{equation*}
\pi_{1}=\frac{P_{a}\left(1-P_{b}\right)}{\left(1-P_{a} P_{b}\right)}, \quad \pi_{2}=\frac{\left(1-P_{a}\right)}{\left(1-P_{a} P_{b}\right)\left(2-P_{a}\right)}, \quad \pi_{3}=\frac{\left(1-P_{a}\right)^{2}}{\left(1-P_{a} P_{b}\right)\left(2-P_{a}\right)} . \tag{1.13.28}
\end{equation*}
$$

The average link utilization can be obtained as

$$
\begin{equation*}
\rho=1-\pi_{1}=\frac{\left(1-P_{a}\right)}{\left(1-P_{a} P_{b}\right)} . \tag{1.13.29}
\end{equation*}
$$

The probability that particular burst have $K$ packets is

$$
\begin{equation*}
P_{R}(K)=\left(1-P_{b}\right)\left(P_{b}\right)^{K-1} \quad K \geq 1 \tag{1.13.30}
\end{equation*}
$$

Thus, the average burst length can be obtained as

$$
\begin{equation*}
B L=\sum_{K=1}^{\infty} K P_{R}(K)=\frac{1}{\left(1-P_{b}\right)} \tag{1.13.31}
\end{equation*}
$$

Because of the correlated arrivals in case of bursty traffic, it is expected that the performance of the switch in terms of packet loss probability is expected to be poorer than the random traffic. This will be further investigated in the thesis.

### 1.14 Thesis Organization

The thesis is organized in the following structure. Chapter 2, discusses various loop buffer based switch architectures while considering the advantages of placement of TWCs inside the buffer. In Chapter 3, various limitations of the loop buffer based architecture are discussed. A mathematical model have also been presented to analyze the switch performance in terms of maximum number of allowed re-circulations of the data in the loop buffer. In Chapter 4, modification have been proposed in the architecture which is discussed in chapter 3, to improve its performance in terms of maximum number of allowed re-circulations such that data can remain in the buffer for the longer duration. In Chapter 5, two architectures are presented where large number of packets can be stored. In the first architecture, control will only be be required only at the input of the switch and not inside the buffer. The second architecture, incorporates fiber Bragg gratings (FBGs) and fiber delay lines (FDLs) to resolve contention among packets. This switch architecture has a very simplified structure. In Chapter 6, an architecture is presented where optical reflectors are used in the buffer; this architecture has further simplified buffer structure and can be easily scaled. In Chapter 7, cost analysis of the different architectures have been presented by using fiber-to-chip coupling (FCC) model while considering different models for the cost of the TWC. Chapter 8, discusses the conclusions and findings of the thesis.

## Chapter 2

## WDM Based Optical Packet Switch Architectures: A Comparison

### 2.1 Introduction

This chapter presents the description of fiber loop buffer based photonic packet switch architectures. These architectures use re-circulating type fiber delay lines for the storage of contending packets. Some of these architectures contain tunable wavelength converters (TWCs) inside the buffer, which can also resolve contention among the packets in wavelength domain ${ }^{1}$. This chapter address the major issues like simultaneous read/write operation, dynamic wavelength re-allocation, control unit complexity, buffering capacity and physical loss of the architectures ${ }^{2}$. Finally, effect of these terms is incorporated in the simulation for analyzing the architectures in terms of packet loss probability.

[^0]

Figure 2.1: Schematic of the architecture A1.

### 2.2 Description of Loop Buffer Based Architectures

### 2.2.1 Loop Buffer Based Architecture A1

The initial design was proposed by Bendelli [4]. It consist of $N$ TWCs one at each input, a random wavelength accessible re-circulating loop buffer having semiconductor optical amplifiers (SOAs) as gate switches for the specified number of wavelengths, and $N$ tunable filters, one at each output (Figure 2.1). The TWCs at the inputs of the switch are tuned at every time slot either to place a packet in the loop buffer to avoid contention or to direct them to the appropriate output. For reading/removing a packet from the buffer, the particular SOA gate is switched 'OFF' and the tunable filter (TF) at the output is tuned to the packet wavelength to accept packet from the buffer. The packets from the buffer are broadcast to all the output ports but selected by the desired port only.


Figure 2.2: Schematic of the architecture A2.

### 2.2.2 Description of Loop Buffer Based Architecture A2

The first modified architecture presented in [52] also consist of $N$ TWCs one at each input, a re-circulating loop buffer with buffer SOAs replaced by the TWCs, and at the output $N$ tunable filters are replaced by $N$ fixed filters. In this architecture another modification is done and resulted structure is shown in Figure 2.2 and defined as architecture A2 [60]. Here, the physical loss of the architecture is reduced by replacing the combination of splitter and fixed filter by one arrayed waveguide grating (AWG) de-multiplexer. In splitter and fixed filter combinations, the splitter divides total power in equal parts and fixed filter selects a particular wavelength. The same operation can be performed by AWG de-multiplexer with much less insertion loss. In the modified architecture, for the removal of the packets from the buffer, respective TWC inside the buffer tune the wavelength of the packets as per the routing pattern of the AWG. In both the architectures the TWCs at the inputs are tuned in every time slot to appropriate wavelength either to place a packet in the loop buffer to avoid contention or to direct them to appropriate output port. Packets from all the inputs use WDM technology to share the loop buffer [76]. The number of buffer wavelengths (size of memory) depends on the desired traffic throughput, packet loss probability and various component pa-


Figure 2.3: Schematic of the architecture A3.
rameters [5, 71]. The packet to be buffered is converted to the wavelength available in the buffer; if memory is full (no wavelength is vacant in the buffer) then the packet cannot be stored, and is lost at the input of the switch.

### 2.2.3 Description of Loop Buffer Based Architecture A3

The basic structure of the architecture is similar to architecture A1, except output ports which are connects via buffer (Figure 2.3) [11]. In this architecture, the AWG demultiplexer (AWG-1) is used to separate the buffer wavelengths and the AWG multiplexer (AWG-2) is used to again combine them. In the buffer two SOA gates (SOA-1 and SOA-2) are placed in each branch of the AWGs. SOA-1 acts as a gate between two buffer AWGs (labelled as AWG-1 and AWG-2) and SOA-2 acts as a gate between AWG-1 and $B \times 1$ AWG as shown in the inset (Figure 2.3). In the architecture, once wavelength is assigned by the input TWC, packet will keep on circulating in the loop buffer at the same wavelength, and SOA-1 in the buffer will remain in the 'ON' state and SOA-2 in the 'OFF' state, until it is desired to read out a packet from the loop buffer. For the removal of the packet from the loop buffer, the respective SOA-1 is


Figure 2.4: Schematic of the architecture A4.
turned 'OFF' and SOA-2 is turned 'ON', and this packet is directed towards the output AWG (marked $B \times 1$, AWG in the figure). All the packets appear at the one port of the AWG. From here the multiplexed signals are allowed to pass through the splitter and particular wavelength is selected by the TF which is placed in each branch of the splitter.

### 2.2.4 Description of Loop Buffer Based Architecture A4

In Figure 2.4, a new proposed architecture is shown, which is similar to the architecture A3, except that the buffer SOAs is replaced by the TWCs. In this architecture once the wavelength is assigned by the input TWC, the packet will keep on circulating in the loop buffer at the same wavelength, and TWC inside the buffer corresponding to that wavelength will remain transparent, until it is desired to read out the packet from the loop buffer. For the removal of the packet from the loop buffer, the respective TWC in the loop buffer tunes the wavelength of the packet corresponding to the appropriate output port as per the routing pattern of the $B \times N$ AWG. The connection between two AWG's placed inside the buffer and one AWG placed at the output is shown in


Figure 2.5: Schematic of read/write operation architecture A1.


Figure 2.6: Schematic of read/write operation architecture A2.
inset of (Figure 2.4). In this architecture buffer unit gets simplified because in each branch which connects AWG-1 and AWG-2, one TWC is required as compared to two SOA's in the architecture A3. Similarly at the output unit only one AWG is required in comparison to three components such as AWG, splitter and TF in A3.

In the next sections (2.3 to 2.7) above architectures will be compared in terms of their functionality.

### 2.3 Buffering and Read/Write Operation

In the original design (Figure 2.1), the buffer memory has a word size equal to one cell period. Its capacity corresponds to pre-determined memory positions or number of
buffer wavelengths. A packet is assigned a wavelength not being used by the packets within the buffer by the input TWC. The SOA (Figure 2.1) is made 'ON' to accept the packet in the buffer. In order to read out the packet from the buffer in architecture A1, the packets which are also broadcast to the outputs are selected by the output filter by tuning itself to packet wavelength and the SOA gate corresponding to buffer wavelength is switched 'OFF' to remove the packet from the buffer. It can be observed that writing to same buffer wavelength as being read from, cannot be done simultaneously; it is possible only after two-cell periods. As shown in Figure 2.5, SOA is switched 'OFF' in the slot ' $i$ ' to remove the packet from the buffer at the wavelength $\lambda_{b}$ and in the next slot ' $i+1$ ' packet at the wavelength $\lambda_{b}$ cannot be inserted in the buffer.

In the proposed modification (Figure 2.2), the loop SOAs gates are replaced by TWCs. The buffer TWCs can be tuned to any of the buffer or output wavelengths. As shown in Figure 2.6, a packet at $\lambda_{b}$ is written into buffer, by tuning the input TWC to buffer wavelength $\lambda_{b}$ in the slot ' $i$ '. It takes one cell period for writing a packet. Assuming that contention is only for one slot duration therefore packet also has to be read out form the buffer in the next slot $(i+1)$. This will also be the minimum time for a buffered packet. For the read out operation the buffer TWC is tuned to $\lambda_{\text {out }}$ for removal of packets from the buffer. Packet is read out from the buffer by converting its wavelength to $\lambda_{\text {out }}$. After conversion, as complete packet crosses the TWC, in process of being buffered out, the TWC buffer wavelength $\lambda_{b}$ becomes free (Figure 2.6). Hence the writing of a new packet on this wavelength $\left(\lambda_{b}\right)$ can take place simultaneously in the slot ' $i+1$ ' as a packet from buffer is being read out. There will be no interference between two wavelengths ( $\lambda_{b}$ and $\lambda_{\text {out }}$ ). Due to the similar operation of the architecture A4, simultaneous read/ write operation is also possible in architectures A4. Architecture A3 will not support simultaneous read/write operation like architecture A1.


Figure 2.7: Schematic of dynamic wavelength re-allocation.

### 2.4 Dynamic Wavelength Re-allocation

A minimum channel spacing of six times the maximum data rate has been recommended in literature to minimize the crosstalk [34]. If TWCs are used as a buffer gates, then it will be possible to dynamically modify the channel spacing while packets are circulating in the buffer to minimizing the crosstalk in loop buffer. This will give flexibility of operation by tuning a packet wavelength to any other available wavelength in the buffer. There is a limit on the maximum number of re-circulations [52], and thus, on the maximum time for which a packet can remain in the buffer to resolve an output contention. One of the factors responsible for this limit is crosstalk. The dynamic wavelength re-allocation will reduce the noise due to crosstalk and may in turn result in an increase in maximum buffering time. This wavelength conversion hence reduces the packet loss probability [12]. An example of dynamic wavelength reallocation is shown in Figure 2.7. This operation is possible in architectures A2 and A4 only.


Figure 2.8: Schematic of control unit complexity.

### 2.5 Control Unit Complexity

The control operation of routing, scheduling, data forwarding etc. is implemented electronically and the actual data transmission takes place optically. The tasks assigned to the control unit (Figure 2.8) are header recognition, routing control, tracking buffer status, tracking input/output port status, synchronization of operation of switch components with master clock in reference, communication with other switching nodes, and executing packet-scheduling algorithm etc.. The complexity of the control unit increases with DWDM application where the number of input channels are large and data rates are very high. Therefore, more photonic components will require synchronized control. The modification of introducing TWC gates in place of SOA results in one less dynamic component, i.e., TF at the output block of the switch. The attempt of introducing passive photonic component, i.e., FF in the existing switch architecture yet maintaining the same switch operational characteristics, eases the complexities of the control unit, as there will be less active component to control and synchronize. The control complexity of the architectures A2 is lowest as only two components input and buffer TWCs have to be controlled. The control complexity of the architecture A1 and A4 is moderate as three components input TWCs, buffer SOAs and output TFs in architecture A1 and input, buffer TWCs and output TFs in architecture A4 have to be controlled. The
control unit complexity is high for architecture A3. Here, four components, i.e., input TWCs, two buffer SOAs and TFs at the outputs have to be controlled by the control unit.

### 2.6 Buffering Capacity

For the architectures A1 and A2, buffer capacity $(B)$ can be fully utilized, but for architectures A3 and A4, the buffer capacity is shared by the directly transmitted and buffered packets. Between the architectures A1 and A2, the later utilizes the buffer capacity more effectively, as for this architecture simultaneous read-write operation is possible. This is not possible in architecture A1.

### 2.7 Physical Loss of the Architectures

The physical loss in the architectures has been evaluated by considering the insertion loss of the each device. The loss of the each component is written in the form $A_{i}^{j}$, where $i$ denote the component type and $j$ size of each of component. The switch architectures are divided into three parts for the description of the loss, viz, $A_{i n}$ which includes the loss from switch input to 3 dB coupler input; $A_{\text {out }}$ includes the loss of 3 dB coupler and the components after that in case of direct transmission and $A_{\text {loop }}$ is the loss in the loop for each of the architectures. For all the architectures it is considered that loop loss is compensated by the amplifier gain such that $A_{\text {loop }}+G_{E D F A}=0$ (in dB units).

The numerical values of losses of various components is assumed as given in [40] and shown in Table 2.1. In the Table loss of the demux and mux is represented by a fitted formula which works well for $N \leq 16[40]$. Here, $N$ is the switch size and $B$ is the
buffer capacity. All the losses in this chapter are expressed in dB.
The loss in the architecture A1 can be modeled as,

$$
\begin{align*}
& A_{\text {in }}=A_{T W C}+A_{\text {Com }}^{N \times 1}  \tag{2.7.1}\\
& A_{\text {out }}=A_{3 d B}+A_{\text {Splitter }}^{1 \times N}+A_{T F}  \tag{2.7.2}\\
& A_{\text {loop }}=A_{3 d B}+A_{\text {Demux }}^{1 \times B}+A_{\text {SOA }}+A_{\text {Com }}^{B \times 1}+A_{\text {Iso }}+A_{\text {Fiber }} \tag{2.7.3}
\end{align*}
$$

The typical, numerical values of different losses for $N=4$ and $B=4$, are $A_{\text {in }}=8 \mathrm{~dB}$,

| Symbol | Parameter | Value |
| :--- | :--- | :--- |
| $A_{3 d B}$ | 3 dB Coupler Loss | 3.0 dB |
| $A_{\text {Com }}^{N \times 1}$ | Combiner Loss | $10\left(\log _{10} N\right) \mathrm{dB}$ |
| $A_{\text {Spl }}^{N \times 1}$ Itter | Splitter Loss | $10\left(\log _{10} N\right) \mathrm{dB}$ |
| $A_{\text {Demux }}^{N \times 1}$ | Demux Loss | $1.5\left(\log _{2} N-1\right) \mathrm{dB}$ |
| $A_{M u x}^{N \times 1}$ | Mux Loss | $1.5\left(\log _{2} N-1\right) \mathrm{dB}$ |
| $A_{\text {TWC }}$ | TWC Loss | 2.0 dB |
| $A_{\text {FF }}$ | Fixed Filter Loss | 1.0 dB |
| $A_{\text {SOA }}$ | Insertion Loss of SOA | 1.0 dB |
| $A_{\text {Iso }}$ | Isolator Loss | 0.15 dB |
| $A_{\text {TF }}$ | Loss of Tunable Filter | 2.0 dB |
| $A_{\text {Fiber }}$ | Loss of the Fiber | $0.2 \mathrm{~dB} / \mathrm{km}$ |

Table 2.1: Value of different parameters
$A_{\text {out }}=11 \mathrm{~dB}$ and $A_{\text {loop }}=11.65 \mathrm{~dB}$. The loss of the loop is compensated by the optical amplifier placed in the buffer, thus $G_{1}=11.65 \mathrm{~dB}$, and the packets which pass through the switch suffers only loss of $A_{\text {in }}+A_{\text {out }}=19 \mathrm{~dB}$.

The loss in the architecture A2 can be written as,

$$
\begin{align*}
& A_{\text {in }}=A_{T W C}+A_{C o m}^{N \times 1}  \tag{2.7.4}\\
& A_{\text {out }}=A_{3 d B}+A_{\text {Demux }}^{1 \times N}  \tag{2.7.5}\\
& A_{\text {loop }}=A_{3 d B}+A_{\text {Demux }}^{1 \times B}+A_{T W C}+A_{\text {Com }}^{B \times 1}+A_{\text {Iso }}+A_{\text {Fiber }} \tag{2.7.6}
\end{align*}
$$

Here, the typical values for losses are $A_{\text {in }}=8 \mathrm{~dB}, A_{\text {out }}=4.5 \mathrm{~dB}$ and $A_{\text {loop }}=12.65 \mathrm{~dB}$. Therefore, $G_{2}=12.65 \mathrm{~dB}$ and the packets which pass through the switch suffer a loss of 12.5 dB , which is less as compared to architecture A1.

The loss in the architecture A3 can be formulated as,

$$
\begin{align*}
A_{\text {in }}= & A_{T W C}+A_{\text {Com }}^{N \times 1}  \tag{2.7.7}\\
A_{\text {out }}= & A_{3 d B}+A_{\text {Demux }}^{1 \times B}+A_{\text {Splitter }}^{1 \times 2}+A_{S O A}+A_{M u x}^{1 \times B}+A_{\text {Splitter }}^{1 \times N}  \tag{2.7.8}\\
& +A_{T F} \\
&  \tag{2.7.9}\\
A_{\text {loop }}= & A_{3 d B}+A_{\text {Demux }}^{1 \times B}+A_{\text {Splitter }}^{1 \times 2}+A_{S O A}+A_{M u x}^{B \times 1}+A_{\text {Iso }}+A_{\text {Fiber }}
\end{align*}
$$

Typically, $A_{\text {in }}=8 \mathrm{~dB}, A_{\text {out }}=18 \mathrm{~dB}$ and $A_{\text {loop }}=10.15 \mathrm{~dB}$. Thus $G_{3}=10.15 \mathrm{~dB}$, and hence the packets which pass through the switch suffer a loss of $A_{\text {in }}+A_{\text {out }}-G_{3}=15.85$ dB . Here, $G_{3}$ is subtracted from the total loss, because, the position of the EDFA in
the loop is such that the directly transmitted packets also gets amplified.
Similarly the loss in architecture A4 can be calculated as

$$
\begin{align*}
& A_{\text {in }}=A_{T W C}+A_{\text {Com }}^{N \times 1}  \tag{2.7.10}\\
& A_{\text {out }}=A_{3 d B}+A_{\text {Demux }}^{1 \times B}+A_{T W C}+A_{\text {Splitter }}^{1 \times 2}+A_{\text {Demux }}^{B \times N}+A_{T F}  \tag{2.7.11}\\
& A_{\text {loop }}=A_{3 d B}+A_{\text {Demux }}^{1 \times B}+A_{T W C}+A_{\text {Splitter }}^{1 \times 2}+A_{M u x}^{B \times 1}+A_{\text {Iso }}+A_{\text {Fiber }} \tag{2.7.12}
\end{align*}
$$

The typical, values of the above losses are $A_{\text {in }}=8 \mathrm{~dB}, A_{\text {out }}=11 \mathrm{~dB}$ and $A_{\text {loop }}=11.15$ $d B$. Here, the loss of the loop is compensated by the amplifier placed in the buffer, thus $G_{4}=11.15 \mathrm{~dB}$, and the packets which pass through the switch suffers a loss of $A_{\text {in }}+$ $A_{\text {out }}-G_{4}=7.85 \mathrm{~dB}$, which is lowest among all the architectures under consideration.

### 2.8 Set of Rules

For architecture A1, A2, the switch uses $(B+N)$ wavelengths, where $B$ is the buffer wavelengths, and $N$ is the number of wavelengths used for direct transmission to the output bypassing the fiber loop [54]. Architecture A3 uses $B$ wavelengths only while architecture A4 uses $2 B$ wavelengths.

1. All-optical wavelength converters at the inputs of the switch can be tuned to any of the $(B+N)$ wavelengths (for A1 and A2) or $B$ and $2 B$ wavelengths for architecture A3 and A4 respectively.
2. For architecture A2 and A4, the buffer is such that simultaneously read and write is allowed in the same slot for the same loop buffer wavelength.
3. If there are $i(1 \leq i \leq B)$ packets in the buffer for the output $j$, one of them will be send to the output. If in that slot, there are one or more packets also present at the inputs for the output $j$, then these will be buffered in the loop buffer to the extent allowed by the rules $4-6$. Any left over packets for output $j$ will be dropped.
4. Considering the case when there is no packet in the buffer for the output $j$, but $m$ input lines have packets for that output. Then, one of these $m$ packets is directly sent to output $j$ in A1 and A2. The remaining $m-1$ packets will be buffered in the buffer to the extent allowed by the rules $5-6$. For A3, A4 all the $m$ packets will be put in the buffer to the extent allowed by rule 5-6.
5. Number of packets $X_{j}$ in the buffer for the output $j$ should never be greater than $B$, i.e., $X_{j} \leq B$ for $j=1 \ldots N$.
6. The total number of buffers used should never be greater than $B$, i.e., $\sum X_{j} \leq B$.

### 2.9 Simulation Results

The performance of the switches is measured through simulation. The simulation code is written in MATLAB ${ }^{\circledR}$. The above defined set of rules are used in the simulation. The simulation environment generate discrete events on the basis of random number generation. Hence, to obtain the steady state results the simulation code is run for $2 \times 10^{6}$ times. In the results 'load' and 'load on the system' are used interchangeably. In Figure 2.9, packet loss probability vs. load is plotted for different architectures for
random traffic model. It can be observed from the figure that architecture A2 performs better in comparison to other architectures, and the performance of the architecture A3 is the poorest. At the load of 0.7 the packet loss probability of the architecture A2 is 100 times better than architecture A3. In Figure 2.10, packet loss probability vs. allowed buffer space is plotted at the load of 0.8 for all the architectures. The


Figure 2.9: Packet loss probability vs. load for switch configuration $N=4$ and $B=8$.


Figure 2.10: Packet loss probability vs. allowed buffer space for load $=0.8(N=4)$.
architectures proposed by us A2 and A4 scales better as compared to the architecture A1 and A3. It can be concluded from these figures that the architecture A2 performs better as compared to other architectures. This happens because in architecture A2, simultaneous read/write is allowed unlike architectures A1 and A3, and all the buffer wavelengths are used for the buffering in contrast to architectures A3 and A4, where buffer wavelengths are shared between directly transmitted and buffered packets. The performance of the architectures A2 and A4 are comparable to each other but better than that of A1 and A3. This clearly indicates simultaneous read/write operation have an impact on the switch performance. In Figure 2.11, probability of packet loss


Figure 2.11: Packet loss probability vs. load on the system for different buffer space ( $N$ $=4)$.
vs. load on the system is plotted for architecture A2, A3 and A4. In this figure, we have not considered architecture A1, because the performance of architecture A1 and A3 is nearly same (Figure 2.9 and Figure 2.10). We have selected A3, because this architecture is recently proposed [11]. In the figure, the maximum allowed buffer space for the architecture A3 and A4 is 16 and for the architecture A2 considered to be 8, 10, 12 and 16. It can be seen from the figure, architecture A2 with buffer space 10 gives
the very similar results as architecture A3 for $B=16$. Similarly, architecture A4 with buffer space $B=16$ gives the similar results as architecture A2 with buffer space 12 . In Figure 2.12, probability of packet loss vs. allowed buffer space at different loading


Figure 2.12: Packet loss probability vs. allowed buffer space for architecture A2 ( $N=$ 4).
condition is plotted for architecture A2. Here as expected, probability of packet loss increases as load increases and at the higher loads, there is not enough advantage of increasing the buffer space. At the load of 0.9 , packet loss probability is improved by only factor of 10 by increasing the buffer space from 4 to 16 .

In Figure 2.13, packet loss probability vs. load is plotted for the bursty traffic. In this figure, three architectures A2, A3 and A4 have been compared. Here, for the less bursty traffic $(B L=2)$ performance of architecture A 3 and A 4 is comparable to each other and they performs poorer than architecture A2. With increase in burst length $(B L=4)$, the architectures A3 and A4 performs almost similarly. Still architecture A2 performs better than other architectures.

In Figure 2.14, packet loss probability is plotted vs. load on the system for the


Figure 2.13: Packet loss probability vs. load under bursty traffic condition $(N=4, B$ $=8$ ).


Figure 2.14: Packet loss probability vs. load for different burst length for architecture A2 $(N=4, B=8)$.
architecture A2 at different burst lengths. Here, the packet loss probability increases with burst length. The packet loss probability tends to be same at the higher loads. In


Figure 2.15: Packet loss probability vs. allowed buffer space for different $B L$ and load for A2 $(N=4)$.

Figure 2.15, packet loss probability vs. allowed buffer space is plotted for architecture A2. With increase in burst length, the advantage due to the increase in buffer space is less. It can be observed from the figure that with increase in burst length, packet loss probability increases. It can also be observed in the figure, at the load of 0.9 and burst length $(B L)=4$ the packet loss probability becomes nearly independent of the buffer space. In Figure 2.16, we have compared the required buffer space at different loading conditions to obtain a packet loss probability of $10^{-4}$. Same data have been presented in the Table 2.2. It is clear from the figure as the load increases more buffer space is required to maintain the same packet loss probability. As the data becomes more bursty in nature, comparatively large buffer space is required. This happens because for the larger burst length there is a finite probability that more number of packets arrives for a particular destination, and a major portion of the buffer gets occupied in very short period, and to accommodate packets for the other outputs some additional buffer space
is required. This can also be viewed from the figure for more bursty traffic ( $B L=4$ at the load of 0.9) because of the arrival of the large number of packets for a particular output, there is no advantage of the increasing the buffer space.

| Load | Buffer Space <br> Random Traffic | Buffer Space <br> Bursty Traffic BL=2 | Buffer Space <br> Bursty Traffic BL=4 |
| :---: | :---: | :---: | :---: |
| 0.1 | 2 | 5 | 10 |
| 0.2 | 3 | 7 | 17 |
| 0.3 | 4 | 9 | 23 |
| 0.4 | 4 | 11 | 27 |
| 0.5 | 6 | 14 | 33 |
| 0.6 | 7 | 18 | 42 |
| 0.7 | 10 | 24 | 53 |
| 0.8 | 16 | 37 | 82 |
| 0.9 | 33 | 68 | 157 |

Table 2.2: Comparison of buffer space at different loading condition for different traffic for architecture A2


Figure 2.16: Buffer space vs. load for different traffic conditions for architecture A2.

| Architecture/Operation | A1 | A2 | A3 | A4 |
| :---: | :---: | :---: | :---: | :---: |
| Simultaneous Read/Write | Not Possible | Possible | Not Possible | Possible |
| Wavelength Re-allocation | Not Possible | Possible | Not Possible | Possible |
| Control Complexity | Moderate | Lowest | Highest | Lowest |
| Number of Components | Moderate | Lowest | Highest | Moderate |
| Buffer Utilization | Moderate | Highest | Lowest | Moderate |
| Packet Loss Probability | Moderate | Lowest | Highest | Moderate |

Table 2.3: Comparison of different architectures in terms of functionality

### 2.10 Conclusions

In this chapter, different photonic switch architectures which have re-circulating type buffer structure have been compared. The performance evaluations of the switches are done in terms of their functionality, packet loss probability and effective buffer utilization. The summary of the comparison of different architectures is presented in Table 2.3. We can conclude the following:

1. The placement of TWCs inside the buffer allows simultaneous read/write operation and dynamic wavelength reallocation, which improves the switch performance in terms of packet loss probability.
2. Simultaneous read/write operation has appreciable impact on the switch performance.
3. Packet loss probability heavily depends on the allowed buffer space.
4. As the data becomes more bursty in nature, there is no advantage of increasing the buffer space.
5. At very high loads packet loss probability becomes nearly independent of the buffer space.

## Chapter 3

## Fiber Optic Loop Buffer Switch: Design and Analysis

### 3.1 Introduction

In the previous chapter, various fiber optic loop buffer based switch architectures were discussed, where contention is resolved in time and wavelength domain and it has been found that architecture A2 performs better than all the other discussed architectures. In this chapter, this architecture is further explored. These re-circulating type buffer structure suffers from circulation limit (maximum revolutions that data can take inside the buffer) due to the large loss of the switch. In this chapter, a mathematical model has been developed to obtain maximum number of allowed re-circulations of the data in loop buffer ${ }^{1}$. This model considers three configuration of TWC. The detrimental effect of four-wave mixing is also shown, and other limitation in terms of buffering capability has also been considered ${ }^{2}$. Finally, in a graph of bit rate vs. buffer wavelengths bounded

[^1]

Figure 3.1: Schematic of simplified architecture for one wavelength only.
regions have been identified in which memory can work efficiently.

### 3.2 Physical Layer Design Constraints

The physical layer limitations in the design of any optical packet switch architecture are due to dispersion and attenuation of the signal. Dispersion limits the maximum possible bit rate for a given length. Length of the fiber limits the minimum possible storage in terms of number of bits at a fixed bit rate. This is because length of the fiber cannot be less than minimum possible physical length. Buffer depth (number of wavelengths available in the buffer) is limited by the physical loss, which increases with scaling of buffer and switch size.

### 3.2.1 Minimum Length Constraints

The minimum length of the fiber loop can be calculated by considering single wavelength buffer. Under this assumption, there will be no requirement of the demux and combiner inside the buffer. The devices can be connected as shown in Figure 3.1. The use of EDFA in the loop is optional for single wavelength buffer. If EDFA is used in the buffer, then minimum length of the loop is limited by the length of the EDFA. But if EDFA is
not used in the buffer, then head and tail end fiber lengths of devices which are used to realize the buffer will limit the minimum possible length of the loop buffer. The loss ${ }^{3}$ of the loop, which is expressed in the fractional units for the simplified buffer structure (Figure 3.1) can be evaluated as,

$$
\begin{equation*}
A_{l o o p}^{\min }=A_{3 d B} A_{T W C} A_{I s o}\left(A_{s}\right)^{J} \tag{3.2.1}
\end{equation*}
$$

While assuming that $J$ splices are required to connect these devices. Here, $A_{3 d B}, A_{T W C}$, $A_{\text {Iso }}$ and $A_{s}$ are losses due to 3 dB coupler, tunable wavelength converter, isolator and splice respectively. Although, we call it min loop loss, any loss value higher than this implies a numerical value less than $A_{\text {loop }}^{m i n}$. The loss of the loop is assumed to be compensated by the gain of EDFA i.e.,

$$
\begin{equation*}
A_{\text {loop }}^{\min } G_{\text {loop }}^{\min }=1 \tag{3.2.2}
\end{equation*}
$$

This condition maximizes the SNR and thus allowed more number of re-circulations of the packets in the buffer [41]. Also, $G_{\text {loop }}^{\min }=\exp \left(\mathrm{g} L_{\text {min }}\right)$. Here $g$ is the gain coefficient has unit of per unit length. In reality, one need to vary pumping so that the gain coefficient and hence gain of the amplifier does not change with input signal power. In other words pumping need to be used to compensate for gain saturation. The gain coefficient $g$ can be made constant with bi-directional pumping. We have assumed constant gain by following the gain stabilization as in [8].

Therefore,

$$
\begin{equation*}
L_{\min }=-\frac{\ln \left(A_{l o o p}^{\min }\right)}{g} \tag{3.2.3}
\end{equation*}
$$

[^2]If EDFA is not used then minimum length of the buffer will be decided by the head and tail length of the devices and can be written as

$$
\begin{equation*}
L_{\min }=\sum_{q=1}^{z}\left(h_{q}+t_{q}\right) . \tag{3.2.4}
\end{equation*}
$$

Here $h$ and $t$ is the head and tail length of the devices, while assuming $z$ devices in the buffer. The total minimum length will be given by,

$$
\begin{equation*}
L_{\min }^{T}=\sum_{q=1}^{z}\left(h_{q}+t_{q}\right)+\left[-\frac{\ln \left(A_{\text {loop }}^{m i n}\right)}{g}\right] . \tag{3.2.5}
\end{equation*}
$$

This equation gives the minimum length constraint on the loop. Therefore, length of the loop cannot be less than $L_{\text {min }}^{T}$.

### 3.2.2 Buffer Constraints

In any optical packet switch it is not possible to increase the buffer space arbitrarily, because as the buffer depth increases the maximum number of allowed re-circulations of the data in the buffer decreases. In this sub-section buffer constraint analysis is presented.

### 3.2.2.1 Loss analysis

For the mathematical ease, switch can be divided into three parts as input unit, buffer unit and output unit. The loss of input unit which consists of TWCs and combiner is given by

$$
\begin{equation*}
A_{i n}=A_{T W C} A_{C o m}^{i n} \tag{3.2.6}
\end{equation*}
$$

The loss of loop buffer can be calculated by breaking the loop into two parts. Let us consider loss from input of the 3 dB coupler to entry port of EDFA to be $A_{1}$ and that from the EDFA output to the input of 3 dB coupler to be $A_{2}$. The $A_{1}$ and $A_{2}$ are given by

$$
\begin{equation*}
A_{1}=A_{3 d B} A_{D e m u x} A_{T W C} A_{C o m}^{b}\left(A_{s}\right)^{5} A_{F 1} \tag{3.2.7}
\end{equation*}
$$

and

$$
\begin{equation*}
A_{2}=A_{\text {Iso }}\left(A_{s}\right)^{3} A_{F 2} \tag{3.2.8}
\end{equation*}
$$

Here, $A_{3 d B}, A_{\text {Demux }}, A_{\text {Com }}, A_{T W C}, A_{s}$ and $A_{\text {Iso }}$ are losses due to 3 dB coupler, demultiplexer, combiner and tunable wavelength converter, splice and isolator loss respectively. $A_{F}=A_{F 1} A_{F 2}$ is the total fiber loss, where $A_{F 1}$ is the loss of fiber segment from coupler to EDFA and $A_{F 2}$ is the loss of fiber segment from EDFA to coupler. If data remain in the buffer of $K$ number of re-circulations, then the total loss suffered by packet in the loop buffer can be written as $A_{\text {loop }}=A^{K}$, where $A=A_{1} A_{2}$ is the loss of the loop buffer in one circulation. Similarly the loss of output unit which consist of coupler and AWG demux can be obtained as

$$
\begin{equation*}
A_{\text {out }}=A_{3 d B} A_{\text {Demux }} . \tag{3.2.9}
\end{equation*}
$$

Here, the loss of 3 dB coupler is considered because as data comes out of the loop buffer it again passes through the coupler. By combing all the above losses, total loss of the switch can be written as

$$
\begin{equation*}
A_{T}=A_{\text {in }} A_{\text {loop }} A_{\text {out }} . \tag{3.2.10}
\end{equation*}
$$

As the loss of the buffer unit is compensated by the EDFA, therefore the above equation can be written as,

$$
\begin{equation*}
A_{T}=A_{\text {in }}\left[A^{K} \prod_{q=1}^{K} G_{q}\left(\lambda_{i}\right)\right] A_{\text {out }} . \tag{3.2.11}
\end{equation*}
$$

Here, $G_{q}\left(\lambda_{i}\right)$ is the gain of the amplifier in $q^{t h}$ re-circulations at wavelength $\lambda_{i}$.

### 3.2.2.2 Power analysis

## TWC as a transparent device:

In this sub-section, TWC is assumed as a transparent device means it will tune the wavelength of the incoming signal without affecting the property of the signal.

Power entering the loop buffer for bit $b$ at wavelength $\lambda_{i}$ is given by

$$
\begin{equation*}
P_{s}\left(\lambda_{i}\right)=b P_{i n}\left(\lambda_{i}\right) A_{i n} \quad b \in[0,1] . \tag{3.2.12}
\end{equation*}
$$

The extinction ratio $\epsilon=[P(1) / P(0)]$ is assumed to be infinite.
Considering additive Gaussian noise of the amplifier signal power after first circulation will be

$$
\begin{equation*}
P_{s}\left(\lambda_{i}, 1\right)=P_{s}\left(\lambda_{i}\right) A G_{1}\left(\lambda_{i}\right)+n_{s p}\left(G_{1}\left(\lambda_{i}\right)-1\right) h \nu B_{0} A_{2} . \tag{3.2.13}
\end{equation*}
$$

In the above equation, the second term $\left[n_{s p}\left(G_{1}\left(\lambda_{i}\right)-1\right) h \nu B_{0}\right]$ represents the ASE noise power added to the signal in the first circulation [43]. Considering the fact that, the data remain in the buffer for $K$ re-circulations. Then, TWC inside the buffer will remain transparent for first $(K-1)^{\text {th }}$ re-circulations and tunes the wavelength in the
$K^{t h}$ re-circulation. Thus, the power of the signal after $K-1$ and $K$ re-circulations for bit $b$ is given by

$$
\begin{equation*}
P_{s}\left(\lambda_{i}, K-1\right)=P_{s}\left(\lambda_{i}, K-2\right) A G_{K-1}\left(\lambda_{i}\right)+n_{s p}\left[G_{K-1}\left(\lambda_{i}\right)-1\right] h \nu B_{0} A_{2} \tag{3.2.14}
\end{equation*}
$$

and

$$
\begin{equation*}
P_{s}\left(\lambda_{j}, K\right)=P_{s}\left(\lambda_{i}, K-1\right) A G_{K}\left(\lambda_{j}\right)+n_{s p}\left[G_{K}\left(\lambda_{j}\right)-1\right] h \nu B_{0} A_{2} \tag{3.2.15}
\end{equation*}
$$

respectively. In these expressions, indices $i$ and $j$ are used for buffer and directly transmitted wavelengths. The term $P_{s}\left(\lambda_{i}, K-1\right)$ is the signal power just before the 3 dB coupler in the beginning of the $K^{t h}$ re-circulation at wavelength $\lambda_{i}, G_{K}\left(\lambda_{j}\right)$ is the gain of EDFA in $K^{t h}$ re-circulation, at wavelength $\lambda_{j}$ and the term $n_{s p}\left[G_{K}\left(\lambda_{j}\right)-1\right] h \nu B_{0}$ represents the ASE noise power added to the signal in the $K^{\text {th }}$ re-circulation. The power for bit $b$ at the output of switch is

$$
\begin{equation*}
P_{\text {out }}\left(\lambda_{j}, K\right)=P_{s}\left(\lambda_{j}, K\right) A_{\text {out }} . \tag{3.2.16}
\end{equation*}
$$

## TWC as a noisy device:

In this section, TWC is assumed as a noisy device. It means when TWC tunes the wavelength of the incoming signal, noise is added to the signal [28, 29]. Model given in [28] is considered for the TWC noise. In the buffer, packet will keep on revolving on the same wavelength till contention resolves. As wavelength conversion is not required while packet keeps re-circulating in buffer, TWC will not introduce any noise. But, during the read-out/write-in process, the TWC will be doing wavelength conversion; accordingly and it will add noise to the signal.

The power entering into the loop buffer for bit $b$ at the wavelength $\left(\lambda_{i}\right)$ will be given by

$$
\begin{equation*}
P_{s}\left(\lambda_{i}\right)=b P_{i n}\left(\lambda_{i}\right) A_{i n} \chi+N_{i n}\left(\lambda_{i}\right) A_{i n}^{C o m} B_{0} \tag{3.2.17}
\end{equation*}
$$

where,

$$
N_{i n}\left(\lambda_{i}\right)=n_{s p}\left(G_{c}-1\right) h \nu \frac{\Gamma g_{0}}{\Gamma g_{0}-\gamma}\left(1+\frac{\chi}{G_{c}}+\frac{b P_{i n}\left(\lambda_{i}\right) A_{T W C} \chi}{P_{p} G_{c}}\right) .
$$

In the equation 3.2.17, first term is the converted signal power and the second term represents noise due to the wavelengths conversion process [28]. Here, $G_{c}$ is the gain of the SOA used inside TWC and $\chi$ is the conversion efficiency. The term $G_{c}$ and $g_{0}$ are obtained by solving the set of equations given in [28]. The parametric values used in the calculations are defined in Table 3.2. Considering maximum number of allowed re-circulations of the data in the buffer as $K$, the corresponding TWC placed inside the buffer will perform tuning in the $K^{t h}$ re-circulation. Since the TWC will not be tuned till $(K-1)^{t h}$ re-circulation so the power for bit $b$ after first and $K-1$ re-circulations will be

$$
\begin{equation*}
P_{s}\left(\lambda_{i}, 1\right)=P_{s}\left(\lambda_{i}\right) A G_{1}\left(\lambda_{i}\right)+n_{s p}\left[G_{1}\left(\lambda_{i}\right)-1\right] h \nu B_{0} A_{2} \tag{3.2.18}
\end{equation*}
$$

and

$$
\begin{equation*}
P_{s}\left(\lambda_{i}, K-1\right)=P_{s}\left(\lambda_{i}, K-2\right) A G_{K-1}\left(\lambda_{i}\right)+n_{s p}\left[G_{K-1}\left(\lambda_{i}\right)-1\right] h \nu B_{0} A_{2} \tag{3.2.19}
\end{equation*}
$$

respectively.
The signal power after $K$ re-circulations is

$$
\begin{align*}
P_{s}\left(\lambda_{j}, K\right)= & P_{s}\left(\lambda_{i}, K-1\right) \chi A G_{K}\left(\lambda_{j}\right)+n_{s p}\left[G_{K}\left(\lambda_{j}\right)-1\right] h \nu B_{0} A_{2}  \tag{3.2.20}\\
& +N_{K}\left(\lambda_{j}\right) A_{C o m}^{b} A_{2} G_{K}\left(\lambda_{j}\right) B_{0}
\end{align*}
$$

where,

$$
N_{K}\left(\lambda_{j}\right)=n_{s p}\left(G_{c}-1\right) h \nu \frac{\Gamma g_{0}}{\Gamma g_{0}-\gamma}\left(1+\frac{\chi}{G_{c}}+\frac{P_{s}\left(\lambda_{i}, K-1\right) A_{s} \chi}{P_{p} G_{c}}\right)
$$

is the noise generated in the $K^{t h}$ re-circulations due to the wavelength conversion process. $A_{s}=A_{3 d B} A_{\text {Demux }} A_{T W C}$ is loss between input of 3 dB coupler to TWC. The power for bit $b$ at the output of switch is

$$
\begin{equation*}
P_{\text {out }}\left(\lambda_{j}, K\right)=P_{s}\left(\lambda_{j}, K\right) A_{\text {out }} . \tag{3.2.21}
\end{equation*}
$$

The above equations can be simplified by assuming the fact that the gain of the EDFA is flat with respect to wavelengths in the region of interest (1530-1570 nm), and in the loop, automatic gain control scheme is assumed [8], and hence constant gain $G$ in each circulation can be considered. Therefore, the equation 3.2.15 can be written in modified form as

$$
\begin{equation*}
P_{s}(K)=P_{s}(K-1) A G\left(\lambda_{i}\right)+n_{s p}(G-1) h \nu B_{0} A_{2} \tag{3.2.22}
\end{equation*}
$$

or

$$
\begin{equation*}
P_{s}(K)=b P_{i n} A_{i n}(A G)^{K}+n_{s p}(G-1) h \nu B_{0} A_{2} F_{K} \tag{3.2.23}
\end{equation*}
$$

Here

$$
F_{K}= \begin{cases}\frac{1-(A G)^{K}}{1-A G}, & A G<1  \tag{3.2.24}\\ K, & A G=1\end{cases}
$$

Similarly the equation 3.2 .20 can be simplified as

$$
\begin{equation*}
P_{s}(K)=b P_{\text {in }} A_{\text {in }} \chi^{2}(A G)^{K}+n_{s p}(G-1) h \nu B_{0} A_{2}\left[F_{(K-1)} A G \chi+1\right]+Z \tag{3.2.25}
\end{equation*}
$$

where,

$$
Z=\left[N_{i n} A_{\text {Com }}^{i n} \chi(A G)^{K}+N_{K} A_{2} G A_{\text {Com }}^{b}\right] B_{0} .
$$

For the maximization of SNR the gain loss product $(A G)$ should be equal to one [41], and considering full conversion i.e. $\chi=1$, the equation 3.2.23 and 3.2.25 can be simplified as,

$$
\begin{align*}
& P_{s}(K)=b P_{i n} A_{i n}+n_{s p}(G-1) h \nu B_{0} A_{2} K  \tag{3.2.26}\\
& P_{s}(K)=b P_{i n} A_{i n}+n_{s p}(G-1) h \nu B_{0} A_{2} K+\left[N_{\text {in }} A_{C o m}^{i n}+N_{K} A_{2} G A_{C o m}^{b}\right] B_{0} \tag{3.2.27}
\end{align*}
$$

respectively. In both the cases power at the output of the switch is

$$
\begin{equation*}
P_{\text {out }}(K)=P_{s}(K) A_{\text {out }} . \tag{3.2.28}
\end{equation*}
$$

## TWC as a regenerative device:

In the third case TWC is assumed as a regenerative device. When the wavelength of the incoming signal is tuned, the signal gets regenerated. This regeneration is assumed
to be 3 R regeneration $[78,79]$. This 3 R regeneration removes the circulation limit and data can remain in the buffer for the longer durations. The performance of the switch under regenerative TWC is explored in next chapter. Therefore it will not be further discussed in this chapter.

### 3.2.2.3 Noise Analysis

The optical amplifiers not only amplify the signal but also add amplified spontaneous emission (ASE) noise to the signal. Due to the square law detection by the photodetector of receiver, various noise components are generated by the beating. These noise components are shot noise, ASE-ASE beat noise, sig-ASE beat noise, ASE-shot beat noise and thermal noise with variances given by [43] $\sigma_{s}^{2}, \sigma_{s p-s p}^{2}, \sigma_{s i g-s p}^{2}, \sigma_{s-s p}^{2}$ and $\sigma_{t h}^{2}$ respectively. These noise variances for bit ' $b$ ', after performing $K$ re-circulations, are given by:

$$
\begin{align*}
\sigma_{s}^{2} & =2 q R P(K) B_{e},  \tag{3.2.29}\\
\sigma_{s p-s p}^{2} & =2 R^{2} P_{s p}^{2}(K)\left(2 B_{o}-B_{e}\right) \frac{B_{e}}{B_{o}^{2}}, \\
\sigma_{s i g-s p}^{2} & =4 R^{2} P(K) \frac{P_{s p}(K) B_{e}}{B_{o}}, \\
\sigma_{s-s p}^{2} & =2 q R P_{s p}(K) B_{e}, \quad \text { and } \\
\sigma_{t h}^{2} & =\frac{4 K_{B} T B_{e}}{R_{L}}
\end{align*}
$$

The expression for $P(K)$ and $P_{s p}(K)$ for TWC as a transparent device will be given by

$$
\begin{equation*}
P(K)=b P_{\text {in }} A_{\text {in }} A_{\text {out }} \quad \text { and } \quad P_{s p}(K)=K n_{s p}(G-1) h \nu B_{0} A_{2} A_{\text {out }} \tag{3.2.30}
\end{equation*}
$$

For TWC as a noisy device, the expression for $P(K)$ will remain same as in equation 3.2.30, and the expression for $P_{s p}(K)$ will be given as

$$
\begin{equation*}
P_{s p}(K)=\left[n_{s p}(G-1) h \nu A_{2} K+N_{\text {in }} A_{\text {Com }}^{i n}+N_{K} A_{2} G A_{\text {Com }}^{b}\right] B_{0} A_{\text {out }} . \tag{3.2.31}
\end{equation*}
$$

The total noise variance for bit ' $b$ ' will be

$$
\begin{equation*}
\sigma^{2}(b)=\sigma_{s}^{2}+\sigma_{s p-s p}^{2}+\sigma_{s i g-s p}^{2}+\sigma_{s-s p}^{2}+\sigma_{t h}^{2} \tag{3.2.32}
\end{equation*}
$$

Under the Gaussian approximation the bit-error rate [43] can be obtained as

$$
\begin{equation*}
B E R=Q\left(\frac{I(1)-I(0)}{\sigma(1)+\sigma(0)}\right) \tag{3.2.33}
\end{equation*}
$$

where $Q(z)$ is known as the error function and is defined as

$$
\begin{equation*}
Q(z)=\frac{1}{\sqrt{2 \pi}} \int_{z}^{\infty} \exp \left(-z^{2} / 2\right) d z \tag{3.2.34}
\end{equation*}
$$

The terms $I(1)=R P(1)$ and $I(0)=R P(0)$ are photocurrent, sampled by the receiver during bit ' 1 ' and bit ' 0 ' respectively, and $R$ is the responsivity of photo-detector.

### 3.2.2.4 $B$ vs. $K$ Relation

In this sub-section relation between $B$ and $K$ is obtained. Under Gaussian approximation the expression for the evaluation of BER is given by [43].

$$
\begin{equation*}
B E R=Q\left(\frac{I(1)-I(0)}{\sigma(1)+\sigma(0)}\right) \tag{3.2.35}
\end{equation*}
$$

or

$$
\begin{equation*}
Q^{-1}[B E R]=\left(\frac{I(1)-I(0)}{\sigma(1)+\sigma(0)}\right) \tag{3.2.36}
\end{equation*}
$$

Applying the values of the different parameters and considering the dominant noise term which is sig-ASE beat noise, the expression will be given by,

$$
\begin{equation*}
Q^{-1}[B E R]=\left(\frac{P(K)}{2 \sqrt{P(K) P_{s p}(K) \frac{B_{e}}{B_{0}}}}\right) \tag{3.2.37}
\end{equation*}
$$

Simple calculation yields

$$
\begin{equation*}
4\left(Q^{-1}[B E R]\right)^{2}=\left(\frac{P_{\text {in }} A_{\text {in }} A_{\text {out }}}{K n_{\text {sp }}(G-1) h \nu B_{e} A_{\text {out }}}\right) \tag{3.2.38}
\end{equation*}
$$

or

$$
\begin{equation*}
K(G-1)=\left(\frac{P_{i n} A_{i n}}{4 n_{s p} h \nu B_{e}\left(Q^{-1}[B E R]\right)^{2}}\right) \tag{3.2.39}
\end{equation*}
$$

At a constant input power the term at the right hand side of the equation becomes a constant. Assuming it to be Const,

$$
\begin{equation*}
K(G-1)=\text { Const } \tag{3.2.40}
\end{equation*}
$$

For large gain, we can approximate as

$$
\begin{equation*}
K \approx \frac{\text { Const }}{G} \tag{3.2.41}
\end{equation*}
$$

The gain of the amplifier placed in the buffer, is a function of buffer size, because buffer size will depends on the size of components used to realize the buffer structure and
thus gain $(G)$ of the amplifier needs to be changed to maintain the condition $A G=1$. Hence,

$$
\begin{equation*}
G=f(B) \tag{3.2.42}
\end{equation*}
$$

Therefore,

$$
\begin{equation*}
K \approx \frac{C o n s t}{f(B)} \tag{3.2.43}
\end{equation*}
$$

Hence, $K$ and $B$ holds inverse relation. The function $f(B)$ can be obtained through the interpolation of data as presented in section 3.5.

### 3.2.2.5 Effect of Four-Wave mixing

In the optical communication system, as the power of the signal increases, the nonlinear effects start to dominate and effect the system performance adversely. In this section, affect of FWM on the system is presented. In deriving the expression for power generation due to FWM, a few assumptions have been made, which can be further explored in $[30,74]$. The major assumptions are 1) it is assumed that FWM components do not interact within EDFA and 2) also there is no interaction between FWM and ASE of the amplifier. Therefore, total noise of the system is modeled as summation of ASE and FWM. In a system with $W$ channels, the total light amplitudes at frequency $f_{F}$ $=f_{p q r}$ is the sum of all the light amplitudes of all the frequency components satisfying the relation,

$$
\begin{equation*}
f_{p q r}=f_{p}+f_{q}-f_{r} \quad(p, q, r=1 \ldots K, p, q \neq r) \tag{3.2.44}
\end{equation*}
$$

Each of these components is generated from different fields that are emitted from different sources. Therefore, there is no correlation between them. So the total FWM power $P_{F W M}$ at frequency $f_{F}$ can be expressed as

$$
\begin{equation*}
P_{F W M}=\sum_{f_{F}=f_{p}+f_{q}-f_{r}} \sum_{f_{q}} \sum_{f_{p}} P_{p q r} \tag{3.2.45}
\end{equation*}
$$

The contribution from $p=r$ and $q=r$ have to be neglected, as they correspond to self phase and cross phase modulations and not for FWM generations [74]. The efficiency of FWM strongly depends on the phase mismatch $\Delta \beta$, which is defined as,

$$
\begin{equation*}
\Delta \beta=\beta\left(\lambda_{p}\right)+\beta\left(\lambda_{q}\right)-\beta\left(\lambda_{r}\right)-\beta\left(\lambda_{F}\right) \tag{3.2.46}
\end{equation*}
$$

In [74], a simplified expression for the power generated due FWM is presented for cascaded EDFA systems. Considering the model, the power of the generated components at frequency $f_{F}$ which corresponds to wavelength $\lambda_{F}$ is

$$
\begin{equation*}
P_{p q r}=\frac{1024 \pi^{6}}{n^{4} \lambda_{F}^{2} c^{2}}\left(d \chi_{n}\right)^{2} \frac{P_{p} P_{q} P_{r}}{A_{e f f}^{2}}\left[\sum_{m=1}^{K} \exp \left(i \sum_{W=1}^{K-1} \Delta \psi^{W}\right) F^{(m)}\right]^{2} . \tag{3.2.47}
\end{equation*}
$$

Here,

$$
\begin{equation*}
\left[F^{(m)}\right]^{2}=\frac{\alpha^{2}}{\alpha^{2}+(\Delta \beta)^{2}}\left[1+\frac{4 e^{-\alpha L} \sin ^{2}\left(\frac{\Delta \beta}{2}\right)}{\left(1-e^{-\alpha L}\right)^{2}}\right] . \tag{3.2.48}
\end{equation*}
$$

The effect of the FWM is most detrimental under the phase matching condition i.e., $\Delta \psi=\Delta \beta L \sim 0$. This condition is easily achieved in the loop buffer, because the length of the loop is few meters and therefore as such there will less effect of dispersion on the signal. Thus equation 3.2 .47 can be further simplified as,

$$
\begin{equation*}
P_{p q r}=\frac{1024 \pi^{6}}{n^{4} \lambda_{F}^{2} c^{2}}\left(d \chi_{n}\right)^{2} \frac{P_{p} P_{q} P_{r}}{A_{e f f}^{2}} K^{2} \tag{3.2.49}
\end{equation*}
$$

$$
d= \begin{cases}3, & f_{p}=f_{q} \neq f_{r}  \tag{3.2.50}\\ 6, & f_{p} \neq f_{q} \neq f_{r}\end{cases}
$$

The above mentioned values of $d$ include all the possible combinations of generated components on different frequencies. But in the loop buffer performance of each channel is measured individually and generally in measurement worst effected signal is considered. Therefore, the above equations 3.2 .49 will be modified as [47],

$$
\begin{equation*}
P_{p q r}=\frac{1024 \pi^{6}}{n^{4} \lambda_{F}^{2} c^{2}} d\left(\chi_{n}\right)^{2} \frac{P_{p} P_{q} P_{r}}{A_{\text {eff }}^{2}} K^{2} A_{\text {out }} \tag{3.2.51}
\end{equation*}
$$

In the equation power of different signal will be given by,

$$
\begin{equation*}
P_{z}=b P_{i n} A_{i n} \quad z \in p, q, r \tag{3.2.52}
\end{equation*}
$$

The degeneracy factors will be given as,

$$
d= \begin{cases}1, & f_{p}=f_{q} \neq f_{r}  \tag{3.2.53}\\ 2, & f_{p} \neq f_{q} \neq f_{r} \\ 2, & f_{p} \neq f_{q} \neq f_{r}=f_{s}\end{cases}
$$

Assuming under the condition, $f_{p} \neq f_{q} \neq f_{r}, c_{1}$ components are generated with degeneracy $d_{1}$; with condition $f_{p} \neq f_{q} \neq f_{r}=f_{s}, c_{2}$ components are generated with degeneracy $d_{2}$ and with $f_{p}=f_{q} \neq f_{r}, c_{3}$ components are generated with degeneracy $d_{3}$. Thus, total numbers of generated components are,

$$
\begin{equation*}
T_{c}=c_{1} d_{1}+c_{2} d_{2}+c_{3} d_{3} \tag{3.2.54}
\end{equation*}
$$

Finally, power of these components using equation 3.2.51 can be evaluated. Since the ASE noise has random phase, it is valid to add FWM spectral components in term of power [30].

$$
\begin{equation*}
P_{T}=P_{S i g}+P_{A S E}+P_{F W M} \tag{3.2.55}
\end{equation*}
$$

Where average FWM power generated for bit one and zero is given by [30]

$$
\begin{align*}
P_{F W M}(1) & =0  \tag{3.2.56}\\
P_{F W M}(0) & =\left[\frac{1}{8} \sum_{p \neq q \neq r} P_{p q r}+\frac{1}{8} \sum_{p=q \neq r} P_{p q r}\right]
\end{align*}
$$

Similarly additional noise variances, generated due to the F.W.M. will be given as [30]

$$
\begin{align*}
& \sigma_{s i g-F W M}^{2}=2 R^{2} P(K) N_{F W M}  \tag{3.2.57}\\
& \sigma_{A S E-F W M}^{2}(1)=4 R^{2} \frac{P_{s p}(K)}{B_{0}} N_{F W M} B_{e} \tag{3.2.58}
\end{align*}
$$

where $N_{F W M}$ will be given by,

$$
N_{F W M}=\left[\frac{1}{8} \sum_{p \neq q \neq r} P_{p q r}+\frac{1}{4} \sum_{p \neq q \neq r=s} P_{p q r}+\frac{1}{4} \sum_{p=q \neq r} P_{p q r}\right]
$$

Similarly noise variance for bit 0 will be given by,

$$
\begin{equation*}
\sigma_{A S E-F W M}^{2}(0)=4 R^{2} \frac{P_{s p}(K)}{B_{0}}\left[\frac{1}{8} \sum_{p \neq q \neq r} P_{p q r}+\frac{1}{4} \sum_{p=q \neq r} P_{p q r}\right] B_{e} \tag{3.2.59}
\end{equation*}
$$

The values of $P(K)$ and $P_{s p}(K)$ is same as in eqn. 3.2.30. The other noise variances will remain same as in equation 3.2.29. Thus, total noise variance for bit $b$ is

$$
\begin{equation*}
\sigma^{2}(b)=\sigma_{s}^{2}+\sigma_{s p-s p}^{2}+\sigma_{s p-s i g}^{2}+\sigma_{s-s p}^{2}+\sigma_{t h}^{2}+\sigma_{s i g-F W M}^{2}+\sigma_{A S E-F W M}^{2} \tag{3.2.60}
\end{equation*}
$$

Thus the BER under the influence of FWM can be evaluated using expression,

$$
\begin{equation*}
B E R=Q\left(\frac{I(1)-I(0)-2 R P_{F W M}(0)}{\sigma(1)+\sigma(0)}\right) \tag{3.2.61}
\end{equation*}
$$

| $\mathbf{P}$ | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | $X$ | $X$ | $X$ | $X$ | 2 | 3 | 4 | 5 |
| 2 | $X$ | $X \cdot \cdots$ | 1 | $X$ | 3 | 4 | 5 | 6 |
| 3 | $X$ | 1 | $2 \cdot \cdot$ | $X$ | 4 | 5 | 6 | 7 |
| 4 | $X$ | $X$ | $X$ | $X \cdot$ | $X$ | $X$ | $X$ | $X$ |
| 5 | 2 | 3 | 4 | $X$ | $\cdot \cdot \cdot$ | 7 | 8 | $X$ |
| 6 | 3 | 4 | 5 | $X$ | 7 | $8 \cdot \cdot$ | $X$ | $X$ |
| 7 | 4 | 5 | 6 | $X$ | 8 | $X$ | $X \cdot$ | $X$ |
| 8 | 5 | 6 | 7 | $X$ | $X$ | $X$ | $X$ | $X \cdot$. |

Figure 3.2: Total number of generated components at frequency 4 in 8 channel system.

The generation of FWM components can be understood from Figure 3.2. The column index ' $p$ ' and row index ' $q$ ' represents the values of $p$ and $q$ respectively as in expression 3.2.44 and corresponding allowed values of index ' $r$ ' are shown. The table has been prepared for eight channels $(W)$ and has values of $r$ leading to FWM output for channel 4. ' $X$ ' entry implies that no permitted value of $r$ exist which will generate FWM output at channel 4. The number of generated components for the condition $p=q \neq r$, are along the diagonal and components for other two conditions $p \neq q \neq r$ and $p \neq q \neq r=s$ for $s=4$ are off diagonal element. The number of waves generated due to the FWM, increases rapidly with number of channels (Table 3.1). For example, in 4 channels system, 5 components are generated at the center frequency and in 8 channels system, 33 components are generated. The strength of each component depends up on phase matching conditions and the effect of FWM is most detrimental under exact phase matching condition. Referring to upper triangle including diagonal elements in table shown in Figure 3.2, $c_{1}=12, d_{1}=2, c_{2}=3, d_{2}=2$ and $c_{3}=3, d_{3}=1$. Thus, total numbers of generated components are $T_{c}=33$. In table shown in Figure 3.2, one need to consider only upper triangular values because lower triangular values can be taken care of with degeneracy factor, e.g. the frequency components can be obtained from the two combinations $f_{7}=f_{6}+f_{3}-f_{2}$ and $f_{7}=f_{3}+f_{6}-f_{2}$. Thus this is equivalent of writing one term with degeneracy 2 .

| Number of buffer wavelengths | Worst affected signal components |
| :---: | :---: |
| 3 | 2 |
| 4 | 5 |
| 5 | 10 |
| 6 | 16 |
| 7 | 24 |
| 8 | 33 |

Table 3.1: Number of generated components on the central frequency for different number of buffer wavelengths

### 3.2.2.6 Dispersion Constraints

The maximum bit rate is limited by the dispersion and can be written as [6]

$$
\begin{equation*}
B_{R} L|D| \Delta \lambda \leq 1 \tag{3.2.62}
\end{equation*}
$$

Here $L$ is the total length traversed by the data in the buffer. $|D|$ is the second order dispersion coefficient and $\Delta \lambda$ is the spectral source width. In terms of loop length $L_{\text {loop }}$ the total traversed length $(L)$ can be written as $L=K L_{\text {loop }}$. Here $K$ is the number of re-circulations of the data in the buffer with $K_{\max }=B$. The length of the fiber loop can be evaluated from the formula

$$
\begin{equation*}
L_{\text {loop }}=\frac{c b_{n}}{n B_{R}} \tag{3.2.63}
\end{equation*}
$$

Here $c$ is the speed of light, $b_{n}$ is number of equivalent bits in one packet slot which are to be stored in the fiber loop, $n$ is the refractive index and $B_{R}$ is the bit rate. After combining eq. 3.2.62 and 3.2.63, it can be deduced that the maximum possible storage in terms of number of bits is

$$
\begin{equation*}
b_{n}=\frac{n}{B c|D| \Delta \lambda} \tag{3.2.64}
\end{equation*}
$$

| Symbol | Parameter | Value |
| :--- | :--- | :--- |
| $R$ | Responsivity | $1.28 \mathrm{Amp} / \mathrm{Watts}$ |
| $n_{s p}$ | Population inversion factor | 1.2 |
| $h$ | Planck's Constant | $6.6 \times 10^{-34} \mathrm{~J}-\mathrm{s}$ |
| $c$ | Speed of Light | $3 \times 10^{8} \mathrm{~m} / \mathrm{s}$ |
| $B_{e}$ | Electrical Bandwidth | 10 GHz |
| $B_{o}$ | Optical Bandwidth | 20 GHz |
| $\epsilon$ | Extinction Ratio | Infinite |
| $q$ | Electronic Charge | $1.6 \times 10^{-19} \mathrm{Coulomb}$ |
| $R_{L}$ | Load Resistance | $300 \Omega$ |
| $T$ | Temperature | 300 K |
| $K_{B}$ | Boltzmann Constant | $1.38 \times 10^{-23} \mathrm{~J} / \mathrm{K}$ |
| $A_{3 d B}$ | 3 dB Coupler Loss | 3.4 dB |
| $A_{C o m}$ | Combiner Loss $(W \times 1)$ | $10\left(\mathrm{Log}_{10} W\right) \mathrm{dB}$ |
| $A_{S p l i t t e r}$ | Splitter Loss $1 \times W)$ | $10\left(\mathrm{Log}_{10} W\right) \mathrm{dB}$ |
| $A_{D e m u x}$ | Demux Loss $(1 \times W)$ | $1.5\left(\mathrm{Log}_{2} W-1\right) \mathrm{dB}$ |
| $A_{T W C}$ | TWC Loss | 2 dB |
| $A_{F F}$ | Fixed Filter Loss | 1 dB |
| $A_{s}$ | Splice Loss | 0.2 dB |
| $A_{F 1}=\mathrm{A}_{F 2}=\alpha$ | Fiber Loss | $0.2 \mathrm{~dB} / \mathrm{km}$ |
| $A_{\text {Iso }}$ | Isolator Loss | 0.15 dB |
| $A_{e f f}$ | Effective Area of the Fiber | $100 \mu \mathrm{~m}^{2}$ |
| $L_{B P F}$ | Band Pass Filter Loss | 1.0 dB |
| $\Delta \lambda$ | Source Spectral Width | 0.2 nm |
| D | Second Order Dispersion Coeff. | $50 \mathrm{ps} / \mathrm{nm}-\mathrm{km}$ |
| n | Refractive index of fiber | 1.54 |
| $\chi_{n}$ | $3^{r d}$ Non-linear Susceptibility | $4 \times 10^{-15} \mathrm{esu}$ |
| $\Gamma$ | Confinement Factor | 1 |
| $\gamma$ | Scattering Loss | $1000 / \mathrm{m}$ |
| $P_{p}$ | Pump Power | 10 mW |

Table 3.2: Value of different parameters

### 3.3 Analysis of the Switch

For switch size $N=4$ and $B=4$, directly used wavelengths ranges from 1550.12 nm to 1552.52 nm , and corresponding buffer wavelengths are from 1534.25 nm to 1536.61 nm . Similarly for the higher values of $N$ and $B$ the wavelengths selection can be done by following the ITU-T grid with a channel spacing of the 0.8 nm . The values of the different parameters used in the calculations are shown in Table 3.2. Since loop buffer is considered with capacity $B=4,8$, and 16 , the gain of the EDFA has to be modified to maintain the condition $A G=1$ inside the loop buffer. The gains for different buffer capacities have been computed by considering the loss through each component of the loop. The corresponding doped fiber length shown in Table 3.3 have been taken from the literature [19].

| Buffer capacity (B) | Gain (G) | Length of EDFA |
| :---: | :---: | :---: |
| 4 | 16.85 dB | 10 m |
| 8 | 21.75 dB | 11 m |
| 16 | 26.65 dB | 14 m |

Table 3.3: Length of the EDFA to provide the required gain

| $\mathbf{N}$ | $\mathbf{B}$ | $\mathbf{K}$ <br> at $\mathbf{P}=\mathbf{- 1 0 d B m}$ | $\mathbf{K}$ <br> at $\mathbf{P}=\mathbf{- 5 d B m}$ | $\mathbf{K}$ <br> at $\mathbf{P}=\mathbf{3 d B m}$ | $\mathbf{K}$ <br> at $\mathbf{P}=\mathbf{0 d B m}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 4 | 4 | 4 | 10 | 17 | 35 |
| 4 | 8 | 1 | 4 | 6 | 11 |
| 4 | 16 | 1 | 2 | 2 | 4 |
| 8 | 8 | 1 | 2 | 3 | 5 |
| 8 | 16 | 1 | 1 | 1 | 2 |
| 16 | 16 | 1 | 1 | 1 | 1 |

Table 3.4: Maximum number of allowed re-circulations at different power levels (For TWC as a transparent device)

In Table 3.4 and Table 3.5, maximum numbers of allowed re-circulations of the data

| $\mathbf{N}$ | $\mathbf{B}$ | $\mathbf{K}$ <br> at $\mathbf{P}=\mathbf{- 1 0 d B m}$ | $\mathbf{K}$ <br> at $\mathbf{P}=\mathbf{- 5 d B m}$ | $\mathbf{K}$ <br> at $\mathbf{P}=\mathbf{- 3 d B m}$ | $\mathbf{K}$ <br> at $\mathbf{P}=\mathbf{0 d B m}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 4 | 4 | 2 | 8 | 16 | 34 |
| 4 | 8 | 1 | 3 | 5 | 10 |
| 4 | 16 | 1 | 1 | 2 | 4 |
| 8 | 8 | 1 | 1 | 2 | 5 |
| 8 | 16 | 1 | 1 | 1 | 2 |
| 16 | 16 | 0 | 1 | 1 | 1 |

Table 3.5: Maximum number of allowed re-circulations at different power levels (For TWC as a noisy device)

| $\mathbf{D}$ | $\mathbf{B}$ | $\mathbf{K}$ <br> at $\mathbf{P}=\mathbf{- 1 0 d B m}$ | $\mathbf{K}$ <br> at $\mathbf{P}=-\mathbf{5 d B m}$ | $\mathbf{K}$ <br> at $\mathbf{P}=\mathbf{3 d B m}$ | $\mathbf{K}$ <br> at $\mathbf{P}=\mathbf{0 d B m}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 4 | 4 | 4 | 10 | 17 | 30 |
| 4 | 8 | 1 | 4 | 6 | 10 |
| 4 | 16 | 0 | 1 | 1 | 2 |

Table 3.6: Maximum number of allowed re-circulations at different power levels (While considering ASE, FWM noise and transparent TWC)
have been presented for various values of $N, B$ at various input power levels, for TWC as a transparent and noisy device respectively. In Table 3.6, maximum numbers of allowed re-circulations are shown while considering the effect of ASE and FWM noise in the buffer. System model discussed earlier is used for calculating maximum allowed re-circulations. The signal power of each of the channels is assumed to be same. The acceptable BER is considered to be less than $10^{-9}$. In the buffer, two scenarios can arise, in the first scenario, each packet can stay in the buffer for $B$ number of recirculations. This happens when $K \geq B$. In this case, there will be no effect of the circulation limits. In the second case, each packet can stay in the buffer for $K<B$ number of re-circulations. Under severe circulation limit if the condition $B=N K$ is achieved in the buffer, then there will be no advantage of increasing of the buffer space. Once the condition $B=N K$ is achieved, shared buffer scheme behaves like an output
buffer scheme, with buffering of maximum $K$ packets for each output. In general the maximum number of packets $X_{j}$ that can be stored for a particular output port $j$ will be $X_{j}=\min (K, B)$ and total maximum number of packets stored in the buffer is $\sum X_{j}$ $=\min (B, N K)$. The circulation constraint can be relaxed using higher power levels (Table 3.4 and Table 3.5) such that the number of packets $X_{j}$ that can be stored for a particular output port $j$ will be $B$ and also total number of packets stored in the buffer i.e., $\sum X_{j}=B$. It is evident from the Table 3.4 and Table 3.5 as the signal power increases the maximum number of allowed re-circulations of the data inside the buffer increases, but with the increment in the buffering capability, maximum number of allowed circulations decreases. It can be observed form the Tables 3.4 and 3.5, that at the lower power level, there is an effect of the TWC noise, but at the higher power level this effect is negligible. In contrast to this, it can be monitored from Table 3.4 and Table 3.6 that at the lower power level there is no effect of FWM, but at the higher power level the effect of FWM is detrimental. For fixed ' $B$ ', increase in power level leads to increase in FWM. For fixed power level, increase in ' $B$ ' also increases FWM. This is expected as FWM is non-linear effect increasing with number of channels as well as power levels. It is evident from the tables that for the larger values of the $N$ and $B$, there will be no advantage of increasing the signal power. In Figure 3.3, maximum number of allowed circulations is plotted at different power levels while considering the effect of ASE noise and FWM. In this figure, power level is considered in mW to clearly visualize the effect in small power range. It can be clearly observed from the figure that the optimum power level is $1 \mathrm{~mW}(0 \mathrm{dBm})$, because when all the channels are present, the maximum number of allowed circulations are nearly same. The another important conclusion that can be drawn is that for the higher values of $B(>8)$ the optimum power level will be less than 0 dBm , because as the number of signals increases the signal under consideration will be affected by the large number of FWM generated


Figure 3.3: $N=4$ and $B=8$ while number of channels presents in the buffer varying from 5 to 8 .
components (Table 3.1), and as shown in Figure 3.3, the maximum number of allowed circulations will decrease. Therefore there is an upper limit also on the power level of the signal and selection of power level depends on the switch and buffer size.

### 3.4 Design Analysis

In the final switch design following conditions must satisfy,
1)The length of the loop must be greater than the minimum loop length i.e.,

$$
\begin{equation*}
L_{\text {loop }} \geq L_{\text {min }}^{T} \tag{3.4.65}
\end{equation*}
$$

2)The selection of switch size should be such that at least $B \leq N K$. If the condition is satisfied, than search for the minimum power level for which $K \geq B$ while considering the detrimental effect of FWM.


Figure 3.4: Schematic of the bounded regimes.
3)The bit rate should be such that the dispersion relation must be obeyed

$$
\begin{equation*}
B_{R} L|D| \Delta \lambda \leq 1 \tag{3.4.66}
\end{equation*}
$$

where $L=K L_{\text {loop }}$ with $K_{\max }=B$
4)The storage in terms of bits also follows the relation,

$$
\begin{equation*}
b_{n} \leq \frac{n}{B c|D| \Delta \lambda} \tag{3.4.67}
\end{equation*}
$$

These conditions are shown in the Figure 3.4. All the equations are drawn on the logarithmic scale, so they appear as straight line with negative slopes. The lines are not to the scale, but they show the behavior of the constraints equations.

### 3.5 Case Study

In this section a case study has been presented considering $N=4$ and $B=8$. From the minimum length constraints, minimum possible length of the loop is 11 m . This is the length of the EDFA to provide sufficient gain with buffering capacity of 8 (Table 3.3). Referring to Table 3.5 , -10 dBm power level cannot be used because at this power level $B>N K$, and therefore, $B-N K$ buffer space will remain effectively unused. To achieve the condition $B<N K$, minimum power level is -5 dBm and at the power level of 0 dBm the circulation limit can be removed (Table 3.4-3.6). Referring to Figure 3.3 , this is also the maximum power that can be used. Therefore 0 dBm is the optimum power level for this configuration. Using equation 3.2.64, the maximum possible storage is 6458 bits. Therefore for the loop length of the 11 m the maximum possible data rate supported by the memory is 110 Gbps (equation 3.2.63). Assuming minimum storage of 10 bits [6], then the minimum possible data rate supported by the memory is 170 Mbps. The inverse relation between $K$ and $B$ can be obtained as,

The gain for different buffer capacities is shown in Table 3.3. We interpolated the data with three curves under the $95 \%$ confidence bounds. The data is fitted on linear, exponential and quadratic functions.

## Linear Model

$$
\begin{equation*}
G=a_{1} B+b_{1} \tag{3.5.68}
\end{equation*}
$$

we interpolated the data and the obtained values of constant are, $a_{1}=35.16$ and $b_{1}=$ -108.


Figure 3.5: Curve fitting of the models.

## Exponential Model

$$
\begin{equation*}
G=a_{2} \exp \left(b_{2} B\right) \tag{3.5.69}
\end{equation*}
$$

The interpolated values of constant are, $a_{2}=37.56$ and $b_{2}=0.1571$.

## Quadratic Model

$$
\begin{equation*}
G=a_{3} B^{2}+b_{3} B+c_{3} \tag{3.5.70}
\end{equation*}
$$

The interpolated values of the constants are, $a_{3}=1.15, b_{3}=11.5$ and $c_{3}=-15.99$. The fitted curve with different models is shown in Figure 3.5 and quadratic model is very accurate.

Finally, the possible values of constraints on different parameters for the switch size $N$ $=4$ and $B=8$ are:

Minimum power level $=-10 \mathrm{dBm}$,

Optimal power level $=0 \mathrm{dBm}$,
Minimum length of the loop $=11 \mathrm{~m}$,
Maximum storage in terms of number of bits is $=6458$,
Minimum storage considered $=10$ bits,
Maximum possible bit rate $=110 \mathrm{Gbps}$ and
Minimum possible bit rate $=170 \mathrm{Mbps}$.

### 3.6 Conclusions

In this chapter, design modeling of the loop buffer based architecture is presented. It has been found that buffer space cannot be scaled arbitrarily because of physical layer constraints. It is shown that for a specific switch combination $(N, B)$ there are optimal design parameter e.g., for $N=4$ and $B=8$, the minimum power level is -10 dBm and to fully utilized the buffer space minimum power level is 0 dBm . Minimum length of the loop is 11 m and minimum possible storage is of 10 bits and maximum storage of 6548 bits with minimum and maximum possible bit rate as 170 Mbps and 110 Gbps respectively. The discussion clearly suggest that only packet loss probability and average delay should not be considered as good enough parameters for the characterizing switch performance.

## Chapter 4

## Optical Loop Memory Based on Regenerators

### 4.1 Introduction

In the previous chapter, limitations of architectures A2 were discussed and it was inferred that storage time of the packets (number of re-circulations) in the buffer is limited by the ASE (amplified spontaneous emission) noise of the amplifier. The effect of ASE noise becomes more severe with switch size and cannot be diminished using higher power levels due to the detrimental effect of FWM. Thus, available buffer space may not be fully utilized because of the packet re-circulation limits in the buffer. In addition to this, in the networks, signal may pass through a large number of switches, therefore to maintain signal integrity, the regeneration of data is essential. To resolve the above mentioned problems, in this chapter, a regenerator based optical loop memory (architecture A5) ${ }^{1}$ has been presented, where re-circulation limit can be improved using regenerator unit inside the buffer, which regenerates the signal after some fixed number

[^3]

Figure 4.1: Schematic of the architecture A5.
of re-circulations ${ }^{2}$. We have also given an optical regenerators placement scheme in the buffer. An expression is derived, to evaluate the required number of regenerators for different buffer capacity $(B)$ and circulation limits $(K)$. Two set of rules for the switch operations are presented. The first set of rules, evaluate the switch performance under circulation limit without considering any regeneration of the data. Therefore, the performance of both the architectures (A2 and architecture presented in this chapter) is same. The second set of rules considers the effect of the regeneration of data and thus shows the performance of the switch (architecture A5) in presence of regenerators inside the buffer.

### 4.2 Description of the Architecture

In the description, size of the switch is assumed to be $N \times N$ with maximum buffering capacity of $B$ packets. The proposed architecture consist of $N$ tunable wavelength converters (TWCs) one at each input, a re-circulating loop buffer and one $1 \times N$ demux at the output (Figure 4.1). The re-circulating loop comprise of 3 dB coupler, demux,

[^4]

Figure 4.2: Schematic of the control operation.

TWC (denoted by $T$ ), regenerator (denoted by $R$ ), combiner, an EDFA to compensate the loop loss and an isolator ${ }^{3}$. In the figure, $R+T$ denote that in that particular branch of demux both regenerator and a TWC are placed. The number of channels passing through the EDFA will vary in different slots, because in reality traffic arrivals are corelated and composed of 'ON' and 'OFF' periods. In the 'OFF' periods no power is transmitted, therefore large variations in power occurs and change the OSNR drastically due to the variability of the traffic [55]. Therefore, to stabilize the gain, a gain clamping scheme as presented in [49], has been assumed which keeps the gain of the EDFA to a constant value irrespective of the number of channels passing through it.

The complete operation of the switch is controlled by a centralized electronic controller as shown in Figure 4.2. At the input of the switch, a small fraction of power is tapped and after $\mathrm{O} / \mathrm{E}$ conversion, is fed to the electronic control unit where the route identifier circuit identifies the routes (buffer/direct path). In the next step, the write controller decide the tuning wavelengths of the packets by analyzing the buffer status. Then

[^5]

Figure 4.3: Schematic of the wavelength shifting through TWC.


Figure 4.4: Schematic of the cyclic nature of the buffer solid line (wavelength filling in buffer) dotted line (wavelength shifting).
the controller sends an appropriate control signal at right instants to the input/buffer TWCs. The buffer tracking status count the packets stored for each output ports and direct the packets to the regenerators unit. The wavelength counter circuits tracks the status of the wavelength used in the buffer. The circulation count $(K)$ is calculated beforehand and fed to the controller.

The TWCs placed at the input of the switch are tuned in each time slot either to place a packet in the buffer or to direct them to the appropriate output port. The switch uses $(B+N)$ wavelengths in which $B$ is number of buffer wavelengths and $N$ is the number of wavelengths used for direct transmission to the output bypassing the fiber loop. Packets are placed in the buffer by converting the wavelengths of the incoming packets to the available buffer wavelengths. On these buffer wavelengths, packets will keep on circulating in the fiber loop memory till contention resolves. The packets can be read
out from the buffer by tuning their wavelength appropriately by following the routing pattern of AWG demux. The set of rules of the switch (presented in section 4.3.2) ensure that each packet gets regenerated before it crosses the upper circulation limit $(K)$ by any one of the regenerator placed in the buffer. Then by tuning the wavelength of the TWC which is placed after the regenerator, the packet can be placed again in the buffer or can be directed to the output by tuning the wavelength appropriately. The buffer demux have $B$ ports correspond to wavelength ranging from $\lambda_{1}$ to $\lambda_{B}$, and few of these wavelengths are used to guide the packet to the regenerators. The contending packets are placed in the buffer at the available wavelengths ranging from $\lambda_{1}$ to $\lambda_{B}$. In each pass through the TWC the wavelength $\lambda_{i}$, for $2 \leq i \leq B$ gets shifted to its lower adjacent wavelength $\lambda_{i-1}$ or converted to intended output port wavelength $\left(\lambda_{j}\right)$ (Figure 4.3). If packet stays in the buffer, then this shifting will allow the automatic selection of regenerator wavelengths $\left(\lambda_{R}\right)$. In this process, some times packets which do not require regeneration will also get regenerated, but there is no expense if a packet gets regenerated earlier than the circulation limit. This shifting in wavelength will eventually may brings the packet to the wavelength $\lambda_{1}$ and to maintain FIFO, wavelength of this packet can again be converted to $\lambda_{B}$. Thus, the packets stored in the buffer follow the cyclic nature of wavelength conversion process (Figure 4.4). The number of regenerators that have to be placed in the buffer will be decided by the circulation limit such that no packet remains in the buffer for more than $K$ circulations without regeneration. In the loop buffer, $3 R$ regeneration is assumed so that after regeneration the data can stay again in the buffer for $K$ more circulations without regeneration [78, 79]. Hence, multiple regenerations of packets will allow longer duration of the data storage. The number of packets $\left(N_{p}\right)$ that can enter the loop buffer in a single time slot will range from 0 to $N$ with maximum buffering capacity of $B$ packets and the maximum number of allowed circulation for each packet without regeneration as $K$. Required number of


Figure 4.5: Schematic of regenerator placement in the buffer.
regenerator for different buffer sizes and circulation limits is given by $R=\left\lceil\frac{B}{K}\right\rceil$ or 0 whichever is larger.

## Proof:

The port of the demux used in the buffer will range from 1 to $B$ but to include the last circulation in which packet either will leave the buffer and appears at the output of the switch or will be placed at tail of the queue, the indexing is considered to be starts from zero. The regenerators have to be placed in the buffer such that the distance (in terms of number of re-circulations) between consecutive regenerators is less than or equal to $K$, this condition allows the automatic selection of next regenerator before circulation index reaches to zero, as allowed number of circulations are decremented by one in each re-circulation. This happens because in each pass through TWC wavelength $\lambda_{i}$ (say wavelength allowed by the port $i$ of the demux) is shifted to lower adjacent wavelength $\lambda_{i-1}$ and packet is passed by the $(i-1)^{t h}$ port of the demux. Because of the cyclic nature of the buffer, we have to assume a starting point of the queue. Here, we have assumed starting point as port 1 of the demux and we have placed first regenerator at this port at wavelength $\lambda_{1}$. Let, $R$ is the number of regenerators that have to be placed in the buffer, numbered as $N_{1}, N_{2} \ldots$ and $N_{R}$ in Figure 4.5 and distance of the $i^{\text {th }}$ regenerators from starting end (index 0) of the demux represents as $D\left(N_{i}\right)$. Here, the equation for the first regenerator can be written as,

$$
\begin{equation*}
D\left(N_{1}\right)=1 \tag{4.2.1}
\end{equation*}
$$

The above equation between consecutive regenerators can be written as,

$$
\begin{equation*}
D\left(N_{j+1}\right)-D\left(N_{j}\right) \leq K \quad \text { for } \quad 1 \leq j \leq R-1 \tag{4.2.2}
\end{equation*}
$$

Further,

$$
\begin{equation*}
B-D\left(N_{R}\right) \leq K-1 \tag{4.2.3}
\end{equation*}
$$

Adding these equations we get,

$$
\begin{equation*}
B<(R+1) K \quad \text { or } \quad \frac{B}{K}<(R+1) \tag{4.2.4}
\end{equation*}
$$

The required number of regenerators will always take integral values, hence

$$
\begin{align*}
R_{m i n}+1 \geq\left\lceil\frac{B}{K}\right\rceil & \text { if } \quad \frac{B}{K} \neq I  \tag{4.2.5}\\
\quad R_{\min }+1>\frac{B}{K} & \text { if } \quad \frac{B}{K}=I \tag{4.2.6}
\end{align*}
$$

or

$$
\begin{align*}
R_{\min } \geq\left\lceil\frac{B}{K}\right\rceil-1 & \text { if } \quad \frac{B}{K} \neq I  \tag{4.2.7}\\
R_{\min }>\frac{B}{K}-1 & \text { if } \quad \frac{B}{K}=I \tag{4.2.8}
\end{align*}
$$

In the regenerative loop buffer, the first regenerator will be placed on the wavelength $\lambda_{1}$ second on $\lambda_{K+1}$ third on $\lambda_{2 K+1}$ and so on.

| Circulation limit $(\boldsymbol{K})$ | Number of regenerators $(R)$ |
| :---: | :---: |
| 2 | 4 |
| 3 | 2 |
| 4 | 2 |
| 5 | 1 |
| 6 | 1 |
| 8 | 1 |

Table 4.1: Required number of regenerators $R$ for different circulations limit ( $K$ ) for switch configuration $N=4$ and $B=8$

The required number of regenerators for switch configuration, $N=4$ and $B=8$, for different circulations limit $(K)$ is presented in Table 4.1. The power budget analysis for the switch shown in Figure 4.1 is performed in previous chapter. For the switch configuration $N=4$ and $B=8$ at the power level of -5 dBm , the maximum number of allowed circulations is found to be four (Table 3.4 of the previous chapter) and for the further analysis, same data is used in this chapter.

### 4.3 Rule Sets for the Switches

### 4.3.1 Set of Rules for Switch A2

1. All optical wavelength converters at the inputs of the switch can be tuned to any of the $(B+N)$ wavelengths instantaneously.
2. Buffer is such that simultaneously read and write is allowed in the same slot for the same wavelength in the loop buffer.
3. If there are $i(1 \leq i \leq B)$ packets in the buffer for the output $j$, one of them will be send to the output. If in that slot, there are one or more packets also present at the inputs for the output $j$, then these will be buffered in the loop buffer to the
extent allowed by the rules 5-6.
4. Considering the case when there is no packet in the buffer for the output $j$, but $m$ input lines have packets for that output. Then, one of these $m$ packets is directly sent to output $j$. The remaining $m-1$ packets will be buffered in the buffer to the extent allowed by the rules 5-6.
5. Number of packets $X_{j}$ in the buffer for the output $j$ should never be greater than $\min$ of $(K, B)$, i.e., $X_{j} \leq \min (K, B)$ for $j=1 \ldots N$.
6. The total number of buffer used should never be greater than $B$, i.e., $\sum X_{j} \leq B$.

### 4.3.2 Rules Set for Switch A5

1. All optical wavelength converters at the inputs of the switch can be tuned to any of the $(B+N)$ wavelengths instantaneously.
2. Buffer is such that simultaneously read and write is allowed in the same slot for the same wavelength in the loop buffer.
3. If there are $i(1 \leq i \leq B)$ packets in the buffer for the output $j$, one of them will be send to the output. If in that slot, there are one or more packets also present at the inputs for the output $j$, then these will be buffered in the loop buffer to the extent allowed by the rules 6-7. The last packet stored decides the $\operatorname{tail}^{(t)}$ of the circular queue.
4. Considering the case when there is no packet in the buffer for the output $j$, but $m$ input lines have packets for that output. Then, one of these $m$ packets is directly sent to output $j$. The remaining $m-1$ packets will be buffered in the buffer to the
extent allowed by the rules $6-7$. The last packet stored decides the $\operatorname{tail}^{(t)}$ of the circular queue.
5. In each time slot, every wavelength $\lambda_{i}$ for $2 \leq i \leq B$ is shifted to its lower adjacent wavelength $\lambda_{i-1}$ or converted to intended output port wavelength and this process continues in cyclic manner by modifying the head ${ }^{(h)}$ and $\operatorname{tail}^{(t)}$ of the circular queue to take care of gaps in the circular queue due to the departed packets.
6. Controller maintains head ${ }^{(h)}$ and tail ${ }^{(t)}$ wavelength of the circular queue. If $t>h$ then $B-(t-h)$ vacant wavelengths are there. If $h>t$ then $h-t$ vacant wavelengths are there. Number of packets $X_{j}$ in the buffer for the output $j$ should never be greater than $B$, for $j=1 \ldots N$.
7. The total number of buffer used should never be greater than $B$, i.e., $\sum X_{j} \leq B$.
8. In any time slot at most number of packets equal to vacant wavelengths, can be inserted in the buffer.

### 4.4 Simulation Results

The simulation code is written in MATLAB ${ }^{\circledR}$. The above defined set of rules are used in the simulation and the obtained results are shown in subsequent figures. In Figure 4.6, packet loss probability vs. load on the system is plotted. Simulation is performed for the switch configuration $N=4, B=8$ while assuming number of re-circulations to be $K=2,4,6$ and 8 . Here, it can be observed that circulation limit have deep impact on the switch performance. Comparing the data at the load of 0.6 for $K=2$ and 4, the packet loss probability is $10^{-2}$ and $10^{-3}$ respectively while for $K=8$ packet loss
probability is $7 \times 10^{-5}$. This is also evident from the figure, as the circulation limit improves, the packet loss probability improves. In Figure 4.7, packet loss probability


Figure 4.6: Packet loss probability vs. load on the system for architecture A2 with switch size $N=4$ and $B=8$ under different circulation limits for random traffic condition.
vs. load is plotted under bursty traffic conditions while considering burst length ( $B L$ ) as 2 and 4 . Here, two configurations are chosen, in the first configuration no circulation limit is considered, while in the second configuration circulation limit $(K)$ is taken to be four. It can be observed from the figure, as the burst length increases the packet loss probability increases, comparing the data at the load of 0.6 the packet loss probability for $B L=2$ and $B L=4$ is $2 \times 10^{-2}$ and $6 \times 10^{-2}$ respectively for circulation limits of four. Without considering any circulation limit, at the load of 0.6 the packet loss probability for $B L=2$ and $B L=4$ is $2 \times 10^{-4}$ and $1 \times 10^{-2}$ respectively. Comparing Figure 4.6 and Figure 4.7, it can be inferred that, under bursty traffic condition due to the correlated arrivals the packet loss probability is higher in comparison to random traffic conditions.

In Figure 4.8, results are plotted for the random traffic and similar results are plotted in Figure 4.9 for the bursty traffic while considering burst length $(B L)=2$ and $R=$


Figure 4.7: Packet loss probability vs. load on the system for architecture A2 with switch size $N=4$ and $B=8$ with and without circulation limits under bursty traffic condition.


Figure 4.8: Packet loss probability vs. load for switch size $N=4$ and $B=8$ for with and without regenerators under random traffic condition.


Figure 4.9: Packet loss probability vs. load for switch size $N=4$ and $B=8$ for with and without regenerators under bursty traffic condition $(B L=2)$.

0 and 2. The $R=0$ represents the performance of the architecture A2 and $R=2$ represents the performance of the architecture A5. It can be clearly visualized from the figures, that there is significant improvement in the packet loss probability while considering $R=2$ in comparison to $R=0$. Comparing the data for random traffic at the load of 0.6 , the packet loss probability is improved by a factor of 100 . Similar trends are also followed with bursty traffic model as in this arrivals are correlated; therefore improvement in packet loss probability is not sharp as in random traffic. As it can be observed in the Figure 4.9 there is difference in the packet loss probability up to load 0.7 and packet loss probability of both the architectures becomes nearly equal at the load of 0.8.

### 4.5 Conclusions

In this chapter, all optical regenerator based packet switch architecture has been presented, in which data is regenerated after finite duration. This has been found that
using regenerator mechanism inside the buffer, circulation limit can be relaxed. The optimal placements of the regenerators in-side the buffer ensure that the buffer space can be utilized effectively with a few numbers of regenerators.

## Chapter 5

## Multi-Wavelength Optical Packet Switch

In chapter 2, various loop buffer based optical packet switch architecture were discussed, and it was found that architecture A2 performs better than other architectures under consideration. In chapter 3, major limitations of the architecture A2 were detailed, and it was found in chapter 4, that regenerative property of TWC is an essential feature for the optical switching. In architecture A2, controlling is required at the input of the switch as well as in the buffer. In this chapter, two architectures have been presented where in the first architecture ${ }^{1}$, controlling will only be required at the input of the switch (no controlling is required inside the buffer). In the second architecture ${ }^{2}$, controlling is required at the input as well as at the output of the switch, but it has very simplified buffering structure ${ }^{3}$. These architectures are wavelength routed switches in

[^6]

Figure 5.1: Schematic of architecture A6.
which, once the wavelength of the incoming packet is tuned appropriately it will either be directly transmitted to the output port or placed in the buffer, and comes out of the loop buffer after desired amount of delay. ${ }^{4}$

### 5.1 Description of the Architectures

### 5.1.1 Architecture A6

The first of the two architectures is shown in Figure 5.1, which is similar to architectures discussed in previous chapters. This architecture also consist of $N$ tunable wavelength converters (TWCs) one at each input, a recirculating loop buffer and one $1 \times N$ demux at the output [62]. The buffering unit of this architecture is different from architecture A2. In the buffer, splitter and combiner is separated by two band pass filters (BPF) and in between one TWC is placed which acts as wavelength shifter. Wavelengths in the buffer are grouped and number of such groups $G_{p}$ equal to the number of TWCs

[^7]| Routing Pattern |  | Delay in slots |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | 0 | 1 | 2 | .. | $j$ | .... | B |
| $\begin{aligned} & \stackrel{n}{3} \\ & \frac{2}{3} \\ & 0 \end{aligned}$ | 1 | $\lambda_{1}$ | $\lambda_{N+1}$ | $\lambda_{2 N+1}$ |  | $\lambda_{j N+1}$ |  | $\lambda_{\text {BN }+1}$ |
|  | 2 | $\lambda_{2}$ | $\lambda_{N+2}$ | $\lambda_{2 N+2}$ |  | $\lambda^{\prime N+2}$ |  | $\lambda_{B N+2}$ |
|  | 3 | $\lambda_{3}$ |  |  |  |  |  |  |
|  | $\ldots$ | $\ldots$ | .... | .... | .... | $\ldots$ | .... | $\ldots$ |
|  | p | $\lambda_{p}$ | $\lambda_{N+p}$ | $\lambda_{2 N+p}$ |  | $\lambda^{\prime N+p}$ |  | $\lambda_{B N+p}$ |
|  | ... | .... | $\ldots$ | .... | .... | ..... | .... | .... |
|  | $N$ | $\lambda_{N}$ | $\lambda_{2 N}$ | $\lambda_{3 N}$ |  | $\lambda_{(j+1) N}$ |  | $\lambda_{(B+1) N}$ |

Figure 5.2: Schematic of the set of wavelengths used for different outputs.
in the loop buffer $(B)$ plus one i.e., $G_{p}=B+1$. Each wavelength group contains $N$ wavelengths one for each output ports. The total number of wavelengths used by the switch is $(B+1) N$, where $B N$ number of wavelengths are used for the buffering of packets and rest $N$ wavelengths are used for the transfer of packets to different outputs. The BPF placed before the TWC in any branch $j$ of the splitter allows $j^{\text {th }}$ group of wavelengths i.e., $\lambda_{j N+1} \ldots . . \lambda_{(j+1) N}$ to pass through it while BPF after TWC in branch number $j$ of the splitter allows only $(j-1)^{t h}$ group wavelengths i.e., $\lambda_{(j-1) N+1} \ldots . . \lambda_{j N}$. Each of the TWC is capable of switching all the incoming wavelengths simultaneously to the new group of wavelengths [37]. The packets placed in the buffer move from one wavelength to another after each circulation; thus by changing the group in each time slot and finally getting assigned to the output wavelength $\left(\lambda_{1} \ldots . . \lambda_{N}\right)$, which is passed to the appropriate output by the demux. The TWC at the input of the switch tunes the packet wavelength to appropriate group depending on the amount of delay required. The wavelength selection within a group is decided by the output port to which packet is destined. Suppose a packet arrives for the destination $p$ and required amount of delay is $j$ slots, then its wavelength will be tuned to $\lambda_{j N+p}$ at the input of the switch (Figure 5.2).

The functionality of the architecture is detailed by considering $4 \times 4$ switch as shown in Figure 5.3 which shows the wavelength domain picture of the buffer. Let $\left(\lambda_{1} \ldots \lambda_{4}\right)$ are


Figure 5.3: Schematic of wavelength domain of the loop buffer.
the wavelengths that are permitted by output demux to go to output 1 to 4 respectively. In the buffer, group 4 wavelengths $\lambda_{17} \ldots \lambda_{20}$ are converted to $3^{\text {rd }}$ group wavelengths $\lambda_{13} \ldots \lambda_{16}$ respectively by the TWC in branch 4 . TWC in branch 3 converts $\lambda_{13} \ldots \lambda_{16}$ to $\left(\lambda_{9} \ldots \lambda_{12}\right)$ and so on. The TWC in branch 1 will convert $\lambda_{5} \ldots \lambda_{8}$ to $\lambda_{1} \ldots \lambda_{4}$ which causes the packet to be removed from the loop buffer and also being allowed to pass through to the output of the packet switch. The above is depicted pictorially in Figure 5.3. If a packet is to be routed to output port 3 , it will be converted to $\lambda_{3}, \lambda_{7}, \lambda_{11}, \lambda_{15}$ or $\lambda_{19}$ depending on whether we have already $0,1,2,3$, or 4 packets in the buffer i.e., delay of zero, one, two, three, or four slots is required. In this architecture, in place of TWCs, fixed wavelength converters (FWCs) can be used because each TWC tunes to fixed set of wavelength only.


Figure 5.4: Schematic of the proposed architecture A7.

### 5.1.2 Architecture A7

The second architecture (A7) as shown in Figure 5.4 consist of $N$ tunable wavelength converters (TWCs) one at each input, a buffer unit and $N$ tunable filters (TF) one at each output [61]. The physical loss of the passive and active components and segments of the fibers is compensated by the EDFA. Packets from all the inputs use WDM technology to share the buffer. The packets to be buffered are converted to the wavelengths available in the buffer; if the buffer is full then packets cannot be stored and are lost. Considering, $N \times N$ switch with buffering capacity of $N B$ packets. Buffer comprises of $B+1$ number of FBGs and consecutive gratings are separated by fiber delay line of half slot duration. These delay lines provide delay of integral multiple of one slot duration as each packet has to pass through each delay line twice, once in forward direction and once in backward direction after getting reflected from the grating. In the buffer, each FBG reflects a set of wavelengths and each set contains $N$ wavelengths, one corresponding to each output and the total number of sets $(S)$ are equal to the buffer capacity plus one i.e. $S=B+1$. Thus, the total number of wavelengths used by the switch is $T$ $=(B+1) N$. Let $\lambda_{1} \ldots \lambda_{N}$ are direct wavelengths, and buffer wavelengths range from $\lambda_{N+1} \ldots \lambda_{(B+1) N}$ as shown in Figure 5.2. The input TWCs tune the wavelengths of the
incoming packets as per the desired outputs and the required amount of delays (Figure 5.3). These wavelengths are combined at the input of the switch, and appear at the port 2 of the circulator and will be reflected by different gratings (Figure 5.4). The reflected wavelengths get routed towards the outputs and TFs will tune its wavelength to accept the packets correspondingly. Suppose a packet arrives for the destination $p$ and required amount of delay is $j$ slots, then its wavelength will be tuned to $\lambda_{j N+p}$ at the input of the switch. While traversing through the buffer, packet will reach the grating $j$ after $j / 2$ slot duration, where it will get reflected and will be delayed by $j / 2$ slot. Hence, total delay of $j$ slots is obtained and the packet is routed to the appropriate output port through the circulator. Thus in the proposed architecture, once packets are placed in the buffer they will be read out from the buffer automatically after definite amount of delay and for removal of the packet from the buffer no controlling is required. Therefore, the control unit complexity is simplified significantly. In the architecture A7, buffer can be easily scaled with FBG's and small segments of fibers. Thus by adding $K$ gratings, the buffer space for each output can be enhanced by $K$ time slots. But in architecture A6 scaling is relatively complex, here size of splitter, combiner has to be increased by a factor of $K$ and in addition to this $2 K$ band pass filters and $K$ TWCs are also required. But still multi-wavelength support by each device is possible. This is in contrast with most of the output queued OPS systems, where at each output port additional buffer of $K$ slots have to be added. Therefore the hardware complexity reduces to $\Theta(K)$ in comparison to $\Theta(N K)$.

### 5.2 Set of Rules for the Switches A6 and A7

1. All optical wavelength converters at the inputs of the switch can be tuned to any of the $(B+1) N$ wavelengths instantaneously.
2. The buffer is such that simultaneous read and write is allowed in the same slot for the same wavelength in the loop buffer.
3. If there are $i$ packets in the buffer for the output $z$, then these packets will be buffered at wavelength ranges from $\lambda_{N+Z}, \lambda_{2 N+Z} \ldots \lambda_{i N+Z}$ and will be read out from the buffer automatically after definite amount of delay at the wavelength $\lambda_{Z}$ in architecture A6 and in architecture A7, packet will leave the buffer at the same wavelength on which it was placed in the buffer ranging from $\lambda_{N+Z}, \lambda_{2 N+Z} \ldots$ $\lambda_{i N+Z}$. If in that slot, there are one or more packets also present at the inputs of the switch for the output $z$, then at most $(B-i+1)$ packets will be stored in the buffer at wavelengths $\lambda_{i N+Z}, \lambda_{(i+1) N+Z \ldots} \lambda_{B N+Z}$ respectively. All the remaining packets for the output $z$ will be dropped.
4. Considering the case when there is no packet in the buffer for the output $z$, but $m$ input lines have packets for that output. Then, one of these $m$ packets is directly sent to output $z$. The remaining $m-1$ packets will be buffered in the buffer to the extent allowed by the rule 3 on $\lambda_{N+Z}, \ldots, \lambda_{(m-1) N+Z}$ when $m-1 \leq B$ else $\lambda_{N+Z \cdots} \lambda_{B N+Z}$ remaining ( $m-B-1$ ) packets will be dropped.

### 5.3 Queuing Structure

In both of these architectures, separate queue is formed for each output. Therefore, the architecture can be modeled as output queued system. The wavelength domain queuing picture for both the architectures is shown in Figure 5.5 and corresponding Markov chain model for the output queuing structure is shown in Figure 5.6. In the output queue analysis [24], a specific queue is considered for performance analysis. The analytical results for this queue are also valid for all other queues as all of them


Wavelength domain output queue for each output

Figure 5.5: Schematic of the wavelength domain queuing picture.


Figure 5.6: Markov chain model for the output queued systems.
are equivalent to each other. This model assumes identical Bernoulli process where in any time slot, probability of the arrival of packet on a particular input is ' $p$ ' and each packet has equal probability ' $1 / N$ ' of being addressed to any one of outputs. Defining a random variable $X$ as the number of packets arriving for a particular tagged output in a given slot, then the probability that exactly $q$ packets will arrive in a slot is

$$
\begin{equation*}
P(q)={ }^{N} C_{q}\left(\frac{p}{N}\right)^{q}\left(1-\frac{p}{N}\right)^{N-q} \quad \text { where } \quad q=0,1 \ldots N . \tag{5.3.1}
\end{equation*}
$$

Let, if $Q_{i}$ denote the number of packets in the tagged queue at the end of the $i^{t h}$ time slot and $X_{i}$ denotes the number of packets arriving in the $i^{\text {th }}$ slot, then $Q_{i}=\min \left[\max \left(0, Q_{i-1}+X_{i}-1\right), B\right]$

No packet will be transmitted to the tagged output queue if $Q_{i-1}=0$ and $X_{i}=0$ in slot $i$. If in any time slot, $Q_{i-1}+X_{i}-1>B$ then $Q_{i-1}+X_{i}-1-B$, packets will be
lost at the input of the switch. The Markov chain model for the output queued system is shown in the Figure 5.6, and the state transition probability $P_{i j}=\operatorname{Pr}\left[Q_{i}=j \mid Q_{i-1}=i\right]$ can be written as

$$
P_{i j}= \begin{cases}p_{0}+p_{1} & i=0, j=0  \tag{5.3.2}\\ p_{0} & 1 \leq i \leq B, j=i-1 \\ p_{j-i+1} & \max (j-N+1,0) \leq i \leq j-1,1 \leq j \leq B-1 \\ \sum_{m=j-i+1}^{N} p_{m} & j=B, \max (j-N+1,0) \leq i \leq j \\ 0 & \text { otherwise }\end{cases}
$$

The steady state distribution of the Markov chain can be obtained as

$$
\begin{equation*}
\pi P_{i j}=\pi \tag{5.3.3}
\end{equation*}
$$

Where $\pi=\left[\begin{array}{lllll}\pi_{0} & \pi_{1} & \pi_{2} & \ldots & \pi_{B}\end{array}\right]^{T}, \pi_{i}$ is the steady state distribution of the state ' $i$ '. The vector $\pi$ should satisfy the following condition,

$$
\begin{equation*}
\sum_{i=1}^{B} \pi_{i}=1 \tag{5.3.4}
\end{equation*}
$$

The packet success probability can be obtained by dividing $\rho_{0}$ by $\rho$. Here $\rho$ is the offered load. Thus packet loss probability will be,

$$
\begin{equation*}
\operatorname{Pr}(\text { Packet Loss })=1-\frac{\rho_{0}}{\rho} \tag{5.3.5}
\end{equation*}
$$

The results in terms of packet loss probability for both the architectures will be exactly same. Therefore, in the subsequent plots results are shown without specifying architecture A6 and A7. In Figure 5.7, packet loss probability vs. load is plotted for the switch size $N=16$, for buffering capacity varying from 2 to 16 . Here, it can be visualized that as the allowed buffer space increases the packet loss probability also improves. Comparing data at the load of 0.6 , there is tremendous improvement in the packet loss


Figure 5.7: Packet loss probability vs. load for switch size $N=16$.
probability for $B=16$ in comparison to $B=2$. Further, as the load increases the packet loss probability increases sharply, but still using higher buffering capacity ( $B=$ 16), lower packet loss rate can be achieved. In Figure 5.8, scaling effects is shown by considering $N=B$ for values 4,8 and 16. Here, as both $N$ and $B$ increases, packet loss probability improves, because at lower load more buffer space will provide better packet loss probability, but at higher load (0.9-1.0) packet loss probability is nearly same because larger arrival rate of packets which also grows with increase in switch size.

### 5.4 Simulation Results

The simulation code is written in MATLAB ${ }^{\circledR}$. The above defined set of rules are used in the simulation and the obtained results are shown in subsequent figures. In this section, results for the packet loss probability vs. load are plotted for the bursty traffic model. In the simulation size of the switch is assumed to be $N=4$. In the Figure 5.9, buffering capacity of 4 and 8 packets is assumed and burst length of 2 and 4 . It can be


Figure 5.8: Packet loss probability vs. load for switch size $N=B$.
observed from the figure that both buffer space and burst length have significant effect on the overall performance of the switches. The packet loss probability improves with increase in buffer space but it increases with burst length. Here, packet loss probability for $B=8$ and $B L=4$ is nearly same as that of $B=4$ and $B L=2$. In the Figure 5.10, packet loss probability vs. load is plotted for different buffer space at fixed burst length $B L=2$. This figure shows the effect of buffer space on the overall packet loss probability. Comparing the data at the load of 0.6 , for $B=4$ and $B=16$ the packet loss probability improves by a factor 100 with $B=16$ and there is significant difference in the packet loss probability at the lower load. The difference diminishes at the higher load. Comparing Figure 5.8 and Figure 5.9 for the switch configuration $N=4$ and $B$ $=4$ there is tremendous difference in packet loss probability this happens because in random traffic, packet arrives uniformly, but in contrast to this, in bursty traffic there is correlated arrival of packets which causes higher packet loss rate. At the higher loads (0.9 and 1.0), packet loss probability cannot be improved significantly by providing additional buffering capacity, because large number of packets will arrive, which show


Figure 5.9: Packet loss probability vs. load for different buffer space $(B)$ and burst length ( $B L$ ).


Figure 5.10: Packet loss probability vs. load for different buffer space ( $B$ ) and burst length $(B L)=2$.


Figure 5.11: Packet loss probability vs. load for different burst length ( $B L$ )
self similar nature. In the Figure 5.11, packet loss probability vs. load is plotted for different burst length at fixed buffer space $\mathrm{B}=8$. This figure clearly shows that the burst length of the correlated arrivals have significant affects on the overall packet loss probability. At the load of 0.4 , the packet loss probability for $B L=2$ is $5 \times 10^{-4}$ while for $B L=4$ it is $1 \times 10^{-2}$.

### 5.5 Conclusions

In this chapter, two multi-wavelength optical packet switches are presented which have distinct advantages over the architectures proposed in the previous chapters. The architecture A6 utilizes the simultaneous wavelength conversion capability of the TWCs, and thus allows large storage capacity and as per our knowledge, this feature of TWCs is first time used in any OPS architecture. In the architecture A7, buffer is created using segments of fiber and fiber Bragg gratings only. The implication of the FBG in the buffer can set a new dimension in optical packet switch architectures because of
its large wavelength scaling, low insertion loss and dispersion reduction capability. It can also be concluded from the chapter that packet loss probability increases with the increase in the load as well as burst length but it decreases with the increment in buffer space. Therefore, to obtain low packet loss rate under bursty traffic condition large buffer space will be required, and this is possible with multi-wavelength buffering structure. The simple routing procedure and relatively simple structures of the architectures makes them better solutions over the conventional architectures.

## Chapter 6

## AWG and Fiber Delay Lines Based Optical Packet Switch Architecture

### 6.1 Introduction

The architectures discussed in the previous chapters, are broadcast and select type switches in nature. As these architectures use splitter and combiner either at the input/output or in the buffer therefore degradation in the signal power is large and ASE noise of the loss compensating EDFA also accumulates with number of re-circulations and thus architectures suffer from the circulations limits. In this chapter, AWG based optical packet switch architecture is presented, as the insertion loss of the AWG is less in comparison to splitter and combiner. Thus, the architecture doesn't suffer form the circulation limits. The basic components used for the realization of the architecture are optical reflectors, tunable wavelength converters (TWCs), arrayed waveguide grating (AWG) and segments of the fibers ${ }^{12}$. This architecture uses routing pattern of AWG

[^8]

Figure 6.1: Schematic of the architecture A8.
and its symmetric nature, to simplify switch operation significantly. This is also shown, using multi-wavelengths optical reflectors length of delay lines can be reduced to half of its original value. This reduction in length is useful for large size packets where length can grow up-to some kilometers.

### 6.2 Description of the Architecture

The proposed architecture utilizes WDM for the storage of the packets in different modules, collectively called as buffer pool. The number of modules in the buffer pool depends on the desired traffic throughput, packet loss probability and various component parameters $[25,71]$. The packets to be buffered are converted to the wavelengths available in the corresponding loop buffer module; if buffer pool is full then packets cannot be stored and are considered as lost. The architecture (Figure 6.1) consists of both scheduling and switching sections. The core of the scheduling section is a $2 N \times 2 N$ AWG


Figure 6.2: Schematic of type - I buffer module.


Figure 6.3: Schematic of type - II buffer module .
router, and that of switching section is a $N \times N$ AWG router. The upper $N$ ports of the AWG router of the scheduling section ranging from 1 to $N$ used to connect $N$ buffer modules. The lower ports $(N+1$ to $2 N)$ of the AWG acts as actual input/output ports of the switch. The architecture presented here is similar to the architectures presented in $[10,36,45]$. Similarity lies in use of the AWG for scheduling and switching section. But proposed architecture has different buffering structure; either optical reflector with circulator or only pieces of fiber are used in the buffer.

In each module, per output port only one packet can be stored. This packet can be stored on any of the free wavelength available in particular module. Thus, at most $N$ packets can be stored for a particular output port in all the modules and in each module $N$ wavelengths are used. This will allow erasing of $N$ packets in single time slot, one corresponds to each output. If the performance of the switch is optimized for $M$ $(M<N)$ number of modules, then rest of the ports of the AWG, i.e., $N-M$ will be left free. Referring equation 6.2.1, it can be observed that, between consecutive modules, $N-1$ wavelengths are in common. Therefore, in $M$ modules $M+N-1$ wavelengths will be required. The lower $N$ ports (inputs/outputs port of the switch) ranges $N+1$ to $2 N$ can be used for the direct transfer of packets. The lower ports are equipped with TWCs
which tune the wavelengths of the incoming packets as per the desired output ports. In buffer pool, module 1 provides a delay of one slot, module 2 provide a delay of two slots and so on. Thus as per the required amount of delay packets can be placed in different modules. Suppose a packet arrives at the input $i$ and destined for output $j$, and requires a delay of $u$ slots, then packet has to be pushed towards module $u$ connected to the $u^{t h}$ port of the AWG. The packet entering at the input port $i$ can be routed to the output port $u$ of the AWG by following the routing pattern of AWG,

$$
\begin{equation*}
\lambda(i, u)=\lambda_{q} \tag{6.2.1}
\end{equation*}
$$

Where, $\quad q=[1+(i+u-1) \bmod N]$

After the delay of $u$ slots packet will again appear at input of the scheduling AWG and get routed to output $i$ of the scheduling AWG due to its symmetric nature (Figure 6.4 orange and pale yellow shaded region). Packet can be directed to the appropriate output by tuning the wavelength by TWC in switching section. In this architecture, two types of buffer modules are considered (Figure 6.2 and Figure 6.3). In the first type only pieces of fiber are used in the buffer, where length varies from 1 to $M$ slots (Figure 6.2). The second type of buffer module (Figure 6.3) consists of one optical reflector, one circulator and pieces of fiber with length varying from $1 / 2$ to $M / 2$ slots. This reduction in length is useful for large size packets, where buffer delay line length can grow up to some kilometers. Optical reflector used in the different modules can be dielectric mirror, thin film based mirror and fiber Bragg grating (FBG) etc.. The full description of the multi-wavelengths FBG is given in [68], where it is shown that, a large number of wavelengths can be reflected from a single grating. The reflectivity of the each wavelength in the entire reflection band is very high 99.8 percent. The insertion loss of the device is negligible and also isolation is as high as 50 dB . Further

|  |  |  |  |  | Out |  |  |  |  | Wavelengths used for buffer to output transfer |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Pat |  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |  |
| $\begin{aligned} & \text { n } \\ & \text { 艺 } \\ & \text { o } \\ & \underline{I} \end{aligned}$ | 1 | $\lambda_{1}$ | $\lambda_{2}$ | $\lambda_{3}$ | $\lambda_{4}$ | $\lambda_{5}$ | $\lambda_{6}$ | $\lambda_{7}$ | $\lambda_{8}$ |  |
|  | 2 | $\lambda_{2}$ | $\lambda_{3}$ | $\lambda_{4}$ | $\lambda_{5}$ | $\lambda_{6}$ | $\lambda_{7}$ | $\lambda_{8}$ | $\lambda_{1}$ |  |
|  | 3 | $\lambda_{3}$ | $\lambda_{4}$ | $\lambda_{5}$ | $\lambda_{6}$ | $\lambda_{7}$ | $\lambda_{8}$ | $M_{1}$ | $\lambda_{2}$ |  |
|  | 4 | $\lambda_{4}$ | $\lambda_{5}$ | $\lambda_{6}$ | $\lambda_{7}$ | $\lambda_{8}$ | $\lambda_{1}$ | $\lambda_{2}$ | $\wedge_{3}$ |  |
|  | 5 | $\lambda_{5}$ | $\lambda_{6}$ | $\lambda_{7}$ | ${ }_{8}$ | $\lambda_{1}$ | $\lambda_{2}$ | ${ }_{3}$ | $\lambda_{4}$ | Wavelengths used for direct transfer |
|  | 6 | ${ }_{6}$ | $\lambda_{7}$ | $\lambda_{8}$ | $\lambda_{1}$ | $\lambda_{2}$ | ${ }_{3}$ | $\lambda_{4}$ | $\lambda_{5}$ |  |
|  | 7 | ${ }_{7}$ | $\lambda_{8}$ | M | $\lambda_{2}$ | $\lambda_{3}$ | $\lambda_{4}$ | $\lambda_{5}$ | $\lambda_{6}$ |  |
|  | 8 | ${ }_{8}$ | $\lambda_{1}$ | $\lambda_{2}$ | $\lambda_{3}$ | $\lambda_{4}$ | $\lambda_{5}$ | $\lambda_{6}$ | $\lambda_{7}$ |  |

## Wavelengths used for input to buffer transfer

Figure 6.4: Routing pattern of $8 \times 8$ AWG router (Scheduling Section).
the grating is also helpful in dispersion reduction. The dielectric and thin film based mirror are capable of reflecting light up to 99.999 percent [48].

### 6.3 Case Study

The operation of the architecture is explained by considering $2 N=8$ i.e., $4 \times 4$ switch. In Figure 6.4, routing pattern of the scheduling AWG of size $8 \times 8$ is shown and sets of wavelengths used for different types of routing. Here, different modules are connected to upper ports 1-4 only, and port number 5-8 are actual inputs/outputs of the switch. The module which is connected to port 1, 2, 3 and 4 provides the delay of one, two, three and four slots respectively. Referring Figure 6.1 in case of $N=4$, suppose a packet arrives at the input port 7 (scheduling section) for the output port 4 (switching section), and requires a delay of 3 time slots, then its wavelength will tuned to $\lambda_{1}$ as shown in Figure 6.5 and will get routed to output port 3 of the scheduling AWG. In the first type buffer, fiber delay will provide the delay of three slots. In the second type of the buffer modules, while traversing through the buffer packet will reach to the reflector

| Routing Pattern |  | Delay |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | 1 | 2 | 3 | 4 |
| $\begin{aligned} & \text { n } \\ & \text { n } \\ & \underline{I} \end{aligned}$ | 5 | $\lambda_{5}$ | $\lambda_{6}$ | $\lambda_{7}$ | $\lambda_{8}$ |
|  | 6 | $\lambda_{6}$ | $\lambda_{7}$ | $\lambda_{8}$ | $\lambda_{1}$ |
|  | 7 | $\lambda_{7}$ | $\lambda_{8}$ | $\lambda_{1}$ | ${ }_{1}$ |
|  | 8 | $\lambda_{8}$ | $\lambda_{1}$ | $\lambda_{2}$ | ${ }_{3}$ |

Figure 6.5: Schematic of the wavelength routing as per the required amount of delay (Scheduling Section).

| Routing <br> Pattern |  | Out puts |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | 1 | 2 | 3 | 4 |
| $\begin{aligned} & \text { Nㅡㄹ } \\ & \text { 号 } \end{aligned}$ | 1 | $\lambda_{1}$ | ${ }^{\prime}$ | ${ }_{3}$ | $\lambda_{4}$ |
|  | 2 | $\lambda_{2}$ | ${ }^{\prime}$ | $\lambda_{4}$ | $\lambda_{1}$ |
|  | 3 | ${ }^{\prime}$ | $\lambda_{4}$ | $\lambda_{1}$ | $\lambda_{2}$ |
|  | 4 | $\lambda_{4}$ | $\lambda_{1}$ | $\lambda_{2}$ | ${ }_{3}$ |

Figure 6.6: Routing pattern of $4 \times 4$ AWG router (Switching Section).
placed in module 3 after $3 / 2$ slots duration, here it will get reflected and there will be delay of $3 / 2$ more slots. After the delay of three time slots the packet will appear at the input port 3 of the scheduling AWG and get routing to output port 7, due to the wavelength routed nature of the AWG. Thus packet appears at the input 3 of TWC of the switching section which comprises AWG of size $4 \times 4$. Here, by converting its wavelength to $\lambda_{2}$, packet can be directed to the output port 4 (Figure 6.6).

### 6.4 Simulation Results

The simulation code is written in MATLAB ${ }^{\circledR}$. The above defined set of rules are used in the simulation and the obtained results are shown in subsequent figures.

### 6.4.1 Random Traffic Model

In the proposed architecture, separate queue is formed for each output; therefore architecture can be modeled as output queued system. The length of the queue for the each
output port will be decided by the number of modules in the buffer pool with maximum queue length of $N$ packets. In output queued system very low packet loss probability is attainable and these queues are formed in wavelength domain, hence additional hardware is not required. The formulation of the output queued system is described in previous chapter. Using the model results for packet loss probability is shown in Figure 6.7 and Figure 6.8. In the Figure 6.7, the chosen switch configuration is $N=8$ with dif-


Figure 6.7: Packet loss probability vs. load for different number of buffer modules.
ferent number of modules $M$ as 2, 4, 6 and 8 . Here, as expected packet loss probability improves with the number of modules and using more number of modules packet loss probability can be reduced as there is significant difference in packet loss probability for $M=2$ and $M=8$. The only disadvantage of the architecture is that, the buffer and inputs/outputs of the switch are shared from single AWG router $(2 N \times 2 N)$. To get the full advantage of the structure $M_{\max }=N$ and number of inputs/outputs are assumed to be $N$. In the similar context scaling effect of the architecture is shown in Figure 6.8 and the size of the AWG router is considered to be 8,16 and 32 with buffering capacity for a particular output $(M)$ is selected as $N$. It is evident from the figure as the switch
size increases the packet loss probability decreases. It can be observed form the figure, even at the load of 0.7 packet loss probability below $10^{-5}$ is attainable for the switch configuration $N=M=16$.


Figure 6.8: Packet loss probability vs. load for $N=M$.

### 6.4.2 Bursty Traffic Model

In Figure 6.9, packet loss probability vs. load is plotted. Here, the size of the switch is assumed to be $N=8$, the number of considered modules is to be 2, 46 and 8 , and burst length $(B L)$ is 2 . Here, as expected as the number of modules increases, packet loss probability decreases as the packet loss probability at the load of 0.6 for $M=2$ is $10^{-1}$ and for $M=8$ is $10^{-2}$. Thus, the packet loss probability is improved by a factor of 10 . It is also observable that beyond the load of 0.8 there is nearly no advantage gain by increasing the buffer modules. Therefore, to obtain low packet loss probability at the higher loads huge amount of buffering capacity will be required.

In Figure 6.10, packet loss probability vs. load is plotted for different burst lengths


Figure 6.9: Packet loss probability vs. load for different number of buffer modules and burst length $(B L=2)$.


Figure 6.10: Packet loss probability vs. load for different burst length ( $B L$ ).

2, 4, 6 and 8 for $N=8$ and $M=8$. It is evident from the figure, as the burst length increases the packet loss probability increases. At the lower load and for the smaller burst length low packet loss rate is possible but the larger burst length increases the packet loss rate increases drastically. If we look at the figure at the load of 0.8 for the $B L=6$ and 8 , the packet loss rate is nearly same. This happens because at the load of 0.8, a large number of packets arrive and large fraction of the arriving packets are lost at the input of the switch.

### 6.5 Conclusions

The architecture proposed in the chapter is realized using components like optical reflectors, tunable wavelength converters (TWCs), arrayed waveguide gratings (AWGs) and segments of fiber. This architecture uses routing pattern of AWG, and its symmetric nature, to simplify switch operation significantly. This is also shown, using multi-wavelengths optical reflectors length of delay lines can be reduced to half of its original value. In the presented architecture, large number of packets can be stored in a single delay lines fiber and in the buffer controlling of the packets is not required. In OPS architectures the physical limitations would be in the number of components (e.g. SOA, EDFA and Mux etc.) required to build the switch. In the architecture proposed here these limitations are eased as buffer can be created by using very few components only. However, the AWG based architectures cannot be scaled easily as crosstalk level of the AWG is as high as $\sim 30 \mathrm{~dB}$.

## Chapter 7

## Cost Analysis of the Optical Packet Switch Architectures

In this thesis, various optical packet switch architectures are proposed and discussed. These architectures have their advantages over the others as discussed in previous chapters. One of the most important issue is the cost of these architectures. As of now most of the active components are not commercially available. Therefore, cost estimation of the architecture is not straight forward. The first compact model which is helpful in the estimation of the cost of the architectures was proposed by Caenegem [7]. The proposed cost model is based on fiber-to-chip coupling (FCC) which is the number of interconnections to the outer world through the component; where the cost of optical components is obtained by counting the number of FCC. The model assumes fix cost for the passive and active devices. Thus, cost of the TWC which can be tuned to $W$ wavelengths is assumed to be 4 (3 input fibers +1 output fiber). As this model assumes fixed cost, it does not include the wavelength speed-up factor (wavelength conversion range). To incorporate the effect of wavelength conversion, a heuristic cost model is proposed in [35] which assumes linear trend in the cost of the TWCs as the wavelength increases. To generalize the cost model, a cost characterization parameter $(b)$ is included in [15].

The proposed models [15, 35] are heuristic in nature and they don't take into account any realization parameters. However, the cost comparison of the architectures can be done, as same model will be used for all the architectures. In this chapter, an alternative method is proposed to derive the cost model which is found to be similar as in [15] but with different range of $b$. Finally, using the different cost models for various optical devices, optical cost of the all the earlier described architectures have been computed.

### 7.1 Description of FCC Model

The optical components used to realize the architectures are 3 dB coupler, combiner, demux, isolator, EDFA, tunable wavelength converters and optical regenerators etc.. Except TWC and optical regenerators rest of the components are commercially available. These two components are heavily investigated in the recent past and will be commercially available soon. The cost model for the optical components based on FCC which is the number of interconnections to the outer world through the component, where the cost of optical components is obtained by counting the number of FCC [7]. The methodology and optical cost of various components follows form [7]. In the FCC cost analysis, internal structure of the device is not considered here only the input and output number of fibers of the device are counted. Therefore, the cost of the optical components can be written as,

$$
\begin{equation*}
C_{\text {Opticaldevice }}=\text { Input fibers }+ \text { Output fibers } \tag{7.1.1}
\end{equation*}
$$

Therefore, the cost of the demux (Figure 7.1) of size $1 \times N$ will be given by

$$
\begin{equation*}
C_{\text {Denux }}=1+N \tag{7.1.2}
\end{equation*}
$$

## Tunable Wavelength Converters



Figure 7.1: Schematic of the demux

In past, TWCs are heavily investigated and experimental results show that the perfor-


Figure 7.2: Schematic of the TWC
mance of a wavelength converter strongly depends on the input and output wavelength selection. The important techniques to realize wavelength converters are FWM [1], cross-gain modulation (XGM) [72] and cross- phase modulation (XPM) [14]. The major problems encountered in these techniques are; the conversion efficiency of the FWM technique is not very high, in XGM extinction ratio is dip by a large amount and in XPM accurate bias control of SOA is required as they are limited to amplitude modulation format. However, FWM and XGM are considered as promising technologies for wavelength conversion. The cost of the tunable wavelength converter which is SOA based and tunability is achieved by the phenomenon of four-wave mixing. In a TWC with 3 input channels four wave mixing happens and signals at frequencies, $f_{p}, f_{q}$ and $f_{r}$ and will interact and generate signal at frequency satisfying the relation,

$$
\begin{equation*}
f_{p q r}=f_{p}+f_{q}-f_{r} \quad(p, q, r=1 \ldots W, \quad p, q \neq r) \tag{7.1.3}
\end{equation*}
$$

In TWCs tunability is achieved by varying the frequency of the pumping signal. Therefore the cost of the TWC (Figure 7.2) will be given by,

$$
\begin{equation*}
C_{T W C}=3+1=4 \tag{7.1.4}
\end{equation*}
$$

## Optical Regenerators

The optical 3 R regenerators are also under extensive investigation as regeneration of the


Figure 7.3: Schematic of the optical regenerator
data is necessary for long distance communication. In the past, numerous publications reported on $3 R$ regeneration in lab environment as well as in field trial [78, 79]. The schematic of the optical regenerator considered in the paper is shown in Figure 7.3 [17]. The major components of the optical $3 R$ regenerator are coupler, semiconductor optical amplifier based Mach-Zehnder interferometers (SOA+ MZI-1, 2), two DFBLaser diode, two band pass filter, one electrical clock recovery module and one $\mathrm{LinbO}_{3}$ modulator. The tunable delay line (TDL) aligns the timing of the reshaped data to the recovered clock. The cost of the optical regenerators can be written as,

$$
\begin{align*}
& C_{\text {Rege }}= C_{C o u p l e r}+C_{D F B-L D}+C_{S O A+M Z I-1}+C_{D F B-L D}  \tag{7.1.5}\\
&+C_{S O A+M Z I-2}+C_{B P F}+C_{T D L}+C_{M o d} \\
& C_{\text {Rege }}=  \tag{7.1.6}\\
& \\
& \\
& \\
&
\end{align*}
$$

The optical cost of the various devices in terms of FCC is presented in Table 7.1.

| Symbol | Representation | Cost |
| :--- | :--- | :--- |
| $C_{T W C}$ | Cost of the TWC | 4 |
| $C_{\text {Combiner }}^{N \times 1}$ | Cost of the Combiner | $N+1$ |
| $C_{\text {Splitter }}^{N \times 1}$ | Cost of the Splitter | $N+1$ |
| $C_{3 d B}$ | Cost of 3 dB Coupler | 4 |
| $C_{\text {Demux }}^{N \times 1}$ | Cost of the Demux | $N+1$ |
| $C_{M u x}^{1 \times N}$ | Cost of the Mux | $N+1$ |
| $C_{E D F A}$ | Cost of the EDFA | 2 |
| $C_{\text {Iso }}$ | Cost of the Isolator | 2 |
| $C_{\text {Rege }}$ | Cost of the Regenerator | 21 |
| $C_{S O A}$ | Cost of the SOA | 2 |
| $C_{F B G}$ | Cost of the FBG | 2 |
| $C_{A W N}^{N \times N}$ | Cost of the AWG | $2 N$ |
| $C_{F F}$ | Cost of the FF | 2 |
| $C_{T F}$ | Cost of the TF | 2 |
| $C_{\text {Cir }}^{N}$ | Cost of the Circulator | $N$ |
| $C_{F}$ | Cost of the Fiber | 2 |
| $C_{O r}$ | Cost of the Optical reflector | 2 |

Table 7.1: Optical cost of the various devices using FCC method

### 7.2 Description and Shortcomings of the Existing Cost Models

As wavelength converters are not commercially available, the cost of these devices cannot be predicted accurately, few cost models have been presented [7, 15, 35]. As discussed above, in the FCC model, cost of the TWC which can be tuned to $W$ wavelengths is assumed to be 4 (3 input fibers +1 output fiber). As this model assumes fixed cost, it does not include the wavelength speed-up factor. To incorporate the effect of wavelength conversion a heuristic cost model have been proposed in [35] where the cost of
the TWCs is given by the expression,

$$
\begin{equation*}
C_{T W C}=a h \tag{7.2.7}
\end{equation*}
$$

Here, ' $a$ ' is a normalization constant, ' $h$ ' is the conversion range. Thus, the cost of the TWC which can be tuned to ' $W$ ' wavelengths will be given by,

$$
\begin{equation*}
C_{T W C}=a W \tag{7.2.8}
\end{equation*}
$$

The model assumes linear trend in cost with respect to the tunable wavelength range. In [15], a relatively more generalized model have been presented where cost is given as,

$$
\begin{equation*}
C_{T W C}=a h^{b} \tag{7.2.9}
\end{equation*}
$$

Here, ' $a$ ' is a normalization constant, ' $h$ ' is the conversion range and ' $b$ ' is wavelength speed-up characterization parameter which characterizes the cost of the TWC and its values lies between 0.5 to 5 [15]. The cost of the TWCs which can be tuned to $W$ wavelengths will be given by

$$
C_{T W C}= \begin{cases}a W^{b}, & W>1  \tag{7.2.10}\\ a, & W=1\end{cases}
$$

As per the cost model presented in [15] the maximum possible value of ' $a$ ' is one. Therefore, TWCs which can tune to one wavelength only will cost unity. It is also mentioned that the cost of the architecture can be optimized by replacing the full range wavelength converters(FRWCs) by limited range wavelength converters (LRWCs) (Figure 7.4). Assuming each LRWC is capable of tuning $W$ wavelengths then for $T$ wavelengths, $J=T / W$ TWCs will be required. To realize the structure, splitter and combiner are also needed which accounts for an additional cost of $2(J+1)$ using FCC


Figure 7.4: Schematic of realization of FRWC using LRWC.
method (Figure 7.4). Therefore, for the cost optimization the following inequality must be satisfied,

$$
\begin{align*}
& 2[J+1]+J\left(W^{b}\right)<T^{b}  \tag{7.2.11}\\
& 2\left[\frac{T}{W}+1\right]+\frac{T}{W}\left(W^{b}\right)<T^{b} \tag{7.2.12}
\end{align*}
$$

Considering $W=1$ which is one extreme, we get

$$
\begin{equation*}
2[T+1]+T<T^{b} \tag{7.2.13}
\end{equation*}
$$

For the higher values of $T$

$$
\begin{equation*}
3 T<T^{b} \tag{7.2.14}
\end{equation*}
$$

This can be simplified to,

$$
\begin{equation*}
b-1>\lim _{T \rightarrow \infty}\left(\frac{\ln 3}{\ln T}\right) \tag{7.2.15}
\end{equation*}
$$

which after further simplification yields $b>1$. Similarly considering other extreme which is $W=T / 2$, we get

$$
\begin{equation*}
6+2\left(\frac{T}{2}\right)^{b}<T^{b} \tag{7.2.16}
\end{equation*}
$$

Note that this corresponds to $J=2$. For the large values of $T$, the equation can be further simplified as,

$$
\begin{equation*}
\left[1-\frac{1}{2^{b-1}}\right]>\left(\frac{6}{T^{b}}\right) \tag{7.2.17}
\end{equation*}
$$

For large values of $T$

$$
\begin{equation*}
\left[1-\frac{1}{2^{b-1}}\right]>0 \tag{7.2.18}
\end{equation*}
$$

which also yields $b>1$. Thus, for large values of $T$ FRWC are more cost effective over LRWC only when $b<1$. It is mentioned in [6] that if traffic is smoothened at the input of the switch and the access link is slower that the back bone link, then buffer space of 10 for each output port can provide 80 percent throughput. For switch of size $4 \times 4$ and buffering capacity $(B)$ as 10 . Hence, the value of $T$ is $N B=40$. Using this value of $T$, the equations 7.2.13 and 7.2.16 can be written as,

$$
\begin{equation*}
122<\left[40^{b}\right] \tag{7.2.19}
\end{equation*}
$$

and

$$
\begin{equation*}
6+2\left(40^{b}\right)<\left[40^{b}\right] \tag{7.2.20}
\end{equation*}
$$

Assuming, $Y 1=40^{b}, Y 2=2(20)^{b}$ and $Y 3=122$. These equations are plotted in Figure 7.5. From equations 7.2 .19 and 7.2 .20 for $W=1$ and $W=T / 2$ it can be inferred that LRWC are advantageous over FRWC for $b$ greater than $b^{t h}=1.31$ and 1.13 respectively (Figure 7.5) and in between for $W=T / 4$ the minimum value of $b^{t h}$ is 1.124 and as $T$ increases $b^{t h}$ tends towards one. Still, the optimal values of $b$, is greater than one for any value of $N$ and $T$. Therefore, as general rule the allowed range of $b$ should be in between 0.5 and 1 to make FRWC more cost effective over LRWC and not 0.5 to 5 as in [7]. Therefore, cost model is efficient when $b<1$, in that case cost of the


Figure 7.5: Cost vs. $b$ plot.
multi-wavelength TWC will be higher than individual TWC but will be less than the total cost of $W$ TWCs. Hence, the constraints on the cost function can be summarized as,

$$
\begin{equation*}
f(T) \leq J f(W) \tag{7.2.21}
\end{equation*}
$$

$$
\begin{equation*}
f(T)>f(W) \tag{7.2.22}
\end{equation*}
$$

$$
\begin{equation*}
f(0)=0 \tag{7.2.23}
\end{equation*}
$$

Where, $f(\bullet)$ is the generalized cost function of the TWC. Considering the cost function as a power series,

$$
\begin{equation*}
f(X)=\sum_{-\infty}^{\infty} a_{b} X^{b} \tag{7.2.24}
\end{equation*}
$$

where ' $X$ ' is a non-negative integer (number of wavelengths) and ' $b$ ', a real number and ' $a_{b}$ ' is just an arbitrary multiplication constant. Therefore equation 7.2 .21 gives,

$$
\begin{align*}
& \sum_{-\infty}^{\infty} a_{b}\left(T^{b}\right) \leq J \sum_{-\infty}^{\infty} a_{b}\left(W^{b}\right)  \tag{7.2.25}\\
& \sum_{-\infty}^{\infty} a_{b}\left(T^{b}\right)-J \sum_{-\infty}^{\infty} a_{b}\left(W^{b}\right)<0 \tag{7.2.26}
\end{align*}
$$

$$
\begin{equation*}
\sum_{-\infty}^{\infty} a_{b}\left(T^{b}\right)\left(1-\frac{1}{J^{b-1}}\right)<0 \tag{7.2.27}
\end{equation*}
$$

This inequality gives (for an + ve integer value of ' $a_{b}$ ', ' $W$ ' and ' $J$ '), $b<1$ (Figure 7.6). From equation 7.2.22, we get

$$
\begin{align*}
& \sum_{-\infty}^{\infty} a_{b}\left(T^{b}\right)>\sum_{-\infty}^{\infty} a_{b}\left(W^{b}\right)  \tag{7.2.28}\\
& \sum_{-\infty}^{\infty} a_{b}\left(T^{b}\right)\left(1-\frac{1}{J^{b}}\right)>0 \tag{7.2.29}
\end{align*}
$$

The second inequality says that $J>1$, and $b>0$ (Figure 7.6). Combining the inequalities we get,

$$
\begin{equation*}
C_{T W C}(X)=a X^{b} \quad \text { for } \quad 0<b \leq 1 \tag{7.2.30}
\end{equation*}
$$

We defined the cost model with modified range of $b$ as wavelength speed-up model (WSU). There may be other functions like $C(X)=\log _{2}(1+W)$ which will satisfy


Figure 7.6: Possible range of $b$.


Figure 7.7: Cost vs. number of wavelengths for various values of $b$
the above constraints equations $7.2 .21-7.2 .23$. But with number of wavelengths, rise in cost is very slow,e.g., for 32 wavelengths cost will only be 5 units. Therefore this function is not acceptable. In Figure 7.7, cost of the TWC with different tunable range
is plotted for different values of $b$ here for lower value of $b$ like 0.5 cost of TWC is very less and for $b=1$ the cost of the TWCs varies linearly wavelengths. The acceptable range of $b$ is in between 0.7 and 0.9. In this range, cost of the TWC rises gradually with respect to wavelengths and cost of the multi-wavelength TWC which can tune to $W$ wavelengths will be less than the cost of the $W$ TWCs which can tune to one wavelength only.

### 7.3 Cost Estimation of the Architectures

In this section, optical cost of various architectures is computed. The total cost of the various architectures are computed by counting the cost of the all the devices needed to realize each switch structure. The cost of different architectures is computed by breaking the each architecture in three separate units as input, buffer and output where the cost of each unit will be given as $C_{\text {in }}, C_{\text {loop }}$ and $C_{\text {out }}$ respectively. The cost of the architecture A1 can be computed as,

The cost of the input unit which consists of TWCs and combiner can be written as,

$$
\begin{equation*}
C_{i n}=N C_{T W C}^{i n}+C_{C o m}^{N \times 1} \tag{7.3.31}
\end{equation*}
$$

The cost of the output unit which consists of splitter and tunable filter will be given by

$$
\begin{equation*}
C_{o u t}=C_{\text {splitter }}^{1 \times N}+N C_{T F} \tag{7.3.32}
\end{equation*}
$$

Similarly, the cost of the buffer unit will be given by,

$$
\begin{equation*}
C_{\text {loop }}=C_{3 d B}+C_{\text {Demux }}^{1 \times B}+B C_{S O A}+C_{C o m}^{B \times 1}+C_{E D F A}+C_{I s o}+C_{F} . \tag{7.3.33}
\end{equation*}
$$

In the notation, cost of each component is represented as $C_{p}^{q}$ where $p$ represents the component type and $q$ is size/position of the device. In the subsequent cost equations buffer is represented as $b u$. Similarly, the costs of the architecture A2 can be modeled as,

$$
\begin{equation*}
C_{i n}=N C_{T W C}^{i n}+C_{C o m}^{N \times 1} \tag{7.3.34}
\end{equation*}
$$

$$
\begin{equation*}
C_{o u t}=C_{\text {Demux }}^{1 \times N} \tag{7.3.35}
\end{equation*}
$$

$$
\begin{equation*}
C_{\text {loop }}=C_{3 d B}+C_{\text {Demux }}^{1 \times B}+B C_{T W C}^{b u}+C_{C o m}^{B \times 1}+C_{E D F A}+C_{I s o}+C_{F} . \tag{7.3.36}
\end{equation*}
$$

The costs of the architecture A3 is given by the expressions,

$$
\begin{align*}
C_{\text {in }}= & N C_{T W C}^{i n}+C_{\text {Com }}^{N \times 1}  \tag{7.3.37}\\
C_{\text {out }}= & C_{\text {Demux }}^{1 \times N}+C_{\text {Splitter }}^{1 \times N}+N C_{T F}  \tag{7.3.38}\\
C_{\text {loop }}= & C_{3 d B}+C_{E D F A}+C_{\text {Demux }}^{1 \times B}+B\left(C_{\text {Splitter }}^{1 \times 2}+2 C_{S O A}\right)  \tag{7.3.39}\\
& +C_{\text {Mux }}^{B \times 1}+C_{I s o}+C_{F} .
\end{align*}
$$

The costs of the architecture A4 can be expressed as,

$$
\begin{equation*}
C_{i n}=N C_{T W C}^{i n}+C_{C o m}^{N \times 1} \tag{7.3.40}
\end{equation*}
$$

$$
\begin{align*}
C_{o u t}= & C_{\text {Demux }}^{B \times N}+N C_{T F}  \tag{7.3.41}\\
C_{\text {loop }}= & C_{3 d B}+C_{E D F A}+C_{\text {Demux }}^{1 \times B}+B\left(C_{T W C}^{b u}+C_{S p l i t t e r}^{1 \times 2}\right)  \tag{7.3.42}\\
& +C_{M u x}^{B \times 1}+C_{I s o}+C_{F} .
\end{align*}
$$

The costs of the architecture A5 can be formulated as,

$$
\begin{align*}
C_{\text {in }}= & N C_{T W C}^{i n}+C_{C o m}^{N \times 1}  \tag{7.3.43}\\
C_{\text {out }}= & C_{\text {Demux }}^{1 \times N}  \tag{7.3.44}\\
&  \tag{7.3.45}\\
C_{\text {loop }}= & C_{3 d B}+C_{\text {Demux }}^{1 \times B}+B C_{T W C}^{b u}+R C_{\text {Rege }}+C_{C o m}^{B \times 1} \\
& +C_{I s o}+C_{F} .
\end{align*}
$$

The costs of the architecture A6 can be represent as,

$$
\begin{align*}
C_{\text {in }}= & N C_{T W C}^{i n}+C_{C o m}^{N \times 1}  \tag{7.3.46}\\
C_{\text {out }}= & C_{\text {Demux }}^{1 \times N}  \tag{7.3.47}\\
C_{\text {loop }}= & C_{3 d B}+C_{S p l i t t e r}^{1 \times B}+B\left(C_{B P F}+C_{T W C}^{b u}+C_{B P F}\right)  \tag{7.3.48}\\
& +C_{C o m}^{B \times 1}+C_{E D F A}+C_{I s o}+C_{F} .
\end{align*}
$$

The costs of the architecture A7 can be defined as,

$$
\begin{align*}
& C_{\text {in }}=N C_{T W C}^{i n}+C_{C o m}^{N \times 1}  \tag{7.3.49}\\
& C_{\text {out }}=C_{E D F A}+C_{S p l i t t e r}^{1 \times N}+N C_{T F}  \tag{7.3.50}\\
& C_{\text {loop }}=C_{C i r}+B C_{F B G}+(B+1) C_{F} . \tag{7.3.51}
\end{align*}
$$

The costs of the architecture A8 can be calculated as,

$$
\begin{align*}
& C_{A 8}= N C_{T W C}^{S c}+C_{A W G}^{S c}(2 N \times 2 N)+M C_{\text {Module }}+N C_{T W C}^{S w}  \tag{7.3.52}\\
&+C_{A W G}^{S w}(2 N \times 2 N) \\
& C_{\text {Module }}(1)=C_{F}  \tag{7.3.53}\\
&  \tag{7.3.54}\\
& C_{\text {Module }}(2)=C_{C i r}+C_{F}+C_{O r}
\end{align*}
$$

The optical costs of the different components using FCC methods are tabulated in Table 7.1. After applying the cost of the different components the cost of the various architectures will be given by the expressions,

$$
\begin{align*}
& C_{A 1}=N C_{T W C}^{i n}+4 N+4 B+14  \tag{7.3.55}\\
& C_{A 2}=N C_{T W C}^{i n}+B C_{T W C}^{b u}+2 N+2 B+14 \tag{7.3.56}
\end{align*}
$$

$$
\begin{align*}
& C_{A 3}=N C_{T W C}^{i n}+4 N+10 B+15  \tag{7.3.57}\\
& C_{A 4}=N C_{T W C}^{i n}+B C_{T W C}^{b u}+4 N+6 B+11  \tag{7.3.58}\\
& C_{A 5}=N C_{T W C}^{i n}+B C_{T W C}^{b u}+2 N+2 B+21 R+14  \tag{7.3.59}\\
& C_{A 6}=N C_{T W C}^{i n}+\frac{B}{N} C_{T W C}^{b u}+2 N+6 \frac{B}{N}+14  \tag{7.3.60}\\
& C_{A 7}=N C_{T W C}^{i n}+4 N+4 \frac{B}{N}+9  \tag{7.3.61}\\
& C_{A 8}=N C_{T W C}^{S c}+N C_{T W C}^{S w}+6 N+\frac{B}{2 N} C_{M o d u l e} \tag{7.3.62}
\end{align*}
$$

In the next two sections cost of the architectures are evaluated numerically, by considering $N=4$ and $B=8$ using various models.

### 7.4 Cost of the Architectures using FCC Method

In Figure 7.8, the cost of the architectures are evaluated by considering FCC model. The cost of the TWC is assumed to be 4 which is independent of the tunable range of the TWCs. Here, the cost of the architecture A3 is highest (127 units) while the cost of the architecture A7 is lowest (49). The cost of the architecture A3 and A4 is comparable to each other. The FCC cost model does not take into account of tunable


Figure 7.8: Total cost of the various architectures using FCC method.
range of the TWCs, therefore higher cost of the architecture can be considered as direct measure of the number of components or size of the components to realize the switch architecture. It should be noted that more number of components with larger switch size will add to the cost. Here, the cost of the multi-wavelength architectures (A6-A7) is less in comparison to other architectures. Thus, this model predict more accurately the number of components needed to realize the structure rather than the actual cost where characteristics of the components like crosstalk, tunable range, switching time etc., will also play a major role. Still, this model is good enough to roughly estimate the cost of devices as it considers the common parameters (FCC) for the estimation of the cost of the various devices. So if the tunable range of the devices is narrow, then this model can be used as cost predictor.


Figure 7.9: Total cost of the various architectures with WSU model.

### 7.5 Cost of the Architectures using Wavelength Speedup Model (WSU)

In Figure 7.9, the cost of the various architectures are shown using WSU model. This model modifies the cost of the TWC by taking into accounts its tunable range. Here, three values of cost characterization parameter ( $b=0.5,0.7$ and 0.9 ) are considered. For $b=0.5$, the cost of the architecture A3 is highest (123 units) and for the architecture A8 (46 units), it is lowest. The cost of the architecture A4 and A5 becomes comparable to the cost of the architecture A3 due to the inclusion of the wavelength conversion range. Similarly, the cost of the architecture A2 becomes higher than the cost of the architecture A1. With increase in the value of $b$ costs of the architectures increases, due to the higher cost of the TWCs. For the higher value of $b=0.9$, the cost of the architecture A 5 is highest (178 units), because it uses $(B+N)$ TWCs each having tuning range of $(B+N)$ and regenerators which adds to the cost by 21 . It can be observed from the figure that with rise in $b$ the cost of the architectures A6 and A7 rises sharply
because in these two architectures the TWCs at the input of the switch have tunable range of $(B+1) N$ wavelengths. The cost of the architecture A6, at $b=0.7$ is 88 and for $b=0.9$ it is 144 . In architecture A8, tunability of the TWCs is proportional to $N$. Therefore, rise in cost in not that sharp with $b$. The architectures from A6 - A8 have multi-wavelength capability, still their cost is less in comparison of architecture A1 to A5. This model is more accurate in comparison to the earlier one as it account for the tunable range of the devices.

### 7.6 Conclusions

In this chapter, various cost models for the estimation of the cost of the TWCs are discussed with their shortcomings. A modification is done in the existing model to make it more compatible and named as WSU model. The presented model is more accurate than the conventional ones, and the proposed model restrict the values of wavelength speed-up characterization parameter $(b)$ between 0.5 and 1 , which was considered earlier in arbitrary values range of 0.5 to 5 . The comparative study of the architectures is preformed with various TWC models and it was found that the architecture A7 and A8 are the most cost effective.

## Chapter 8

## Conclusions and Future Works

### 8.1 General Conclusions

The optical packet switch is considered as next generation data transfer technology because of its high throughput, low latency, fine granularity and ultimate bandwidth utilization. The lack of commercially viable optical buffering technology imposes a constraint on the commercial development of optical packet switches. Once optical components are available, then the offering of OPS systems can be fully utilized. In this thesis, various optical packet switch architectures were described which can acts as a optical router in core networks. This chapter discusses the major conclusions of the works presented in the thesis.

### 8.2 Advantages of Optical Loop Buffer(OLB)

In this thesis, various optical loop buffer based architectures are presented. The key advantages of OLB are:

1. Delay of the signal placed in the buffer can be varied by changing the number of re-circulations.
2. More than one packets can be stored in single fiber delay lines using WDM technique.
3. Fiber length used to create the buffer is $\operatorname{small}(\backsim 10 \mathrm{~m})$.
4. Control complexity is less.
5. Shared buffer structure is possible.
6. Only single amplifier is good enough for all the channels.

### 8.3 Limitations of Optical Loop Buffer (OLB)

1. ASE noise accumulation limits the maximum number of re-circulation of the data in the buffer.
2. As more than one signals are stored in a single strand of fiber crosstalk between adjacent channels occurs.
3. Due to the presence of more than one signals in the buffer four-wave mixing happens and degrade the quality of the signal.
4. Foot print of the erased signal also acts as crosstalk.
5. Tunable range of devices like SOAs/TWCs has to be large which adds to the design complexity.
6. Large physical loss of the loop degrade the signal quality within few number of re-circulations.

### 8.4 Specific Conclusions

In this thesis various optical loop buffer based architectures were discussed. We started our study with four architectures defined as A1, A2, A3 and A4 in chapter 2 and it was found that implication of the TWCs inside the buffer facilitates simultaneous read/write operation, dynamic wavelength-reallocation and reduction in control points. Due to the stated advantages there is large reduction in packet loss probability and it was found that architecture A2 performs better than other architectures in terms of packet loss probability. In chapter 3, architecture A2 is further explored while considering the detrimental effects of attenuation and dispersion which are physical layer impairments. The detrimental effect of FWM is also shown and it was found that the buffering time of the packets in the buffer is limited by these impairments. Thus, packets can stay in the buffer for the limited number of re-circulations. Finally, it was concluded due to these limitations OPS architecture can work efficiently with-in the bounded regimes. To counteract the problem the placement of regenerator's in-side the buffer was proposed in chapter 4 and it was found that using them buffer capacity can be utilized fully without any circulation limits. This chapter also conclude that to maintain signal integrity the regeneration of the data is essential in OPS architectures as signal may have to pass through a large number of such switches in the optical core networks. The use of regenerators inside the buffer may increase the buffering time of the data by regenerating it inside the buffer. But the structure becomes more complex and costly and still in the buffer each wavelength needs to be controlled separately. In chapter 5, two multiwavelength optical packet switches were presented which have large storing capability. The first of these two architectures A6 utilizes the simultaneous wavelength conversion capability of the TWCs, and thus allows large storage capacity. In the architecture A7 buffer is created using segments of fiber and fiber Bragg gratings only. These two
architecture have potential to perform better than other architecture under bursty traffic condition where large buffer space will be required to obtain low packet loss probability. Finally, we have presented an architecture A8 which is realized using components like optical reflectors, tunable wavelength converters (TWCs), arrayed waveguide gratings (AWGs) and segments of fiber. This architecture uses routing pattern of AWG, and its symmetric nature, to simplify switch operation significantly. This is also shown, using multi-wavelengths optical reflectors length of delay lines can be reduced to half of its original value. In the presented architecture, large number of packets can be stored in a single delay lines fiber and in the buffer controlling of the packets is not required. In the architecture proposed here these limitations are eased as buffer can be created by using very few components only. In chapter 7, cost estimation of the architectures is presented. The cost analysis of the architectures is done using FCC method while for the cost of the TWC various models are considered. In chapter 7, it was found that architecture A7 and A8 have lower cost than other architectures.

### 8.5 Essentials for the OPS architectures

In the course of my thesis duration and while analyzing the work we come across with some essential for the commercial viable optical packet switch which are as:

1. In our opinion the implemental optical packet switch, should be designed in such a way that the use of splitter/combiner can be minimized.
2. The regenerative property of TWC is essential as switch may be cascaded.
3. Multi-wavelength support by each port of the device used to create buffer is essential.
4. The use of multi-wavelength FBGs in realization of buffer can set a new dimension to optical switching.

### 8.6 Future Works

This thesis mainly concentrate on the proposal and design of novel optical packet switch architectures. As with optical packet switches many issues are involved, here we have selected few of them rest of the issues can be a part of further study. In specific, few possible further exploration are:

1. The modeling of the architectures can be re-performed by considering the regenerators mathematical models for 2 R and 3 R regenerators.
2. The performance evaluation of the architectures can be performed with different traffic condition like Pareto etc..
3. The effect of packet priority can be included in the performance evaluation of the architectures.
4. The mathematical model can be redesigned while considering the effect of device crosstalk.
5. The cascadability analysis of the architectures can be preformed.
6. The performance and size of the switches can be optimized by placing them in different networks topologies.
7. The experimental study can be done to verify the models.

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# List of Papers: Accepted and Communicated 

## List of Publications

## Patents:

1. R. Srivastava, R. K. Singh and Y. N. Singh, "WDM optical packet switch incorporating Fiber Bragg Gratings and Circulator," Indian Patent office, patent application no. 2706/DEL/2007 (patent filed).
2. R. Srivastava, R. K. Singh and Y. N. Singh, "All Optical reflectors Based WDM optical Packet Switch," Indian Patent office, patent application no. 2707/DEL/2007 (patent filed).

## Published Papers:

## Journal Papers:

1. Rajat Kumar Singh, Rajiv Srivastava and Yatindra Nath Singh, "Wavelength division multiplexed loop buffer memory based optical packet switch," Optical and Quantum Electronics, Vol. 39, No. 1, pp. 15-34, 2007.
2. Rajiv Srivastava, Rajat Kumar Singh and Yatindra Nath Singh, "Optical loop memory for photonic switching application" Journal of Optical Networking, Vol. 6, No. 4, pp. 341-348, 2007.
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1. Swapnil Shukla, Rajiv Srivastava, Y. N. Singh, "Modelling of fiber loop buffer based switch, " Proc. PHOTONICS Conf. 2004.
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2. Rajiv Srivastava and Yatindra Nath Singh, "Fiber Optic Loop Buffer Switch Incorporating 3R Regeneration," Journal of Optical Switching and Networking, (Under Review).
3. Rajiv Srivastava and Yatindra Nath Singh, "Feedback Fiber Delay Lines and AWG Based Optical Packet Switch Architecture," Journal of Optical Switching and Networking, (Under Review).

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